Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (1/98)
Approved for use through 09/30/2000 OMB 0651-0032
Patent and Trademark Office U S DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-1980

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title: ELECTRO-OPTICAL DEVICE AND DRIVING METHOD FOR THE SAME

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [41]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [20]
4. [X] Oath or Declaration *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. [X] Other: Notice of Change of Address

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment*
Divisional of prior application Serial No. 08/964,028, filed November 4, 1997; which itself is a Divisional of Serial No. 08/766,709, filed December 13, 1996, now U.S. Patent 5,905,555; which is a Divisional of Serial No. 08/542,821, filed October 13, 1995, now U.S. Patent 5,612,799; which is a Divisional of Serial No. 08/224,992, filed April 8, 1994, now U.S. Patent 5,495,353; which is a Divisional of Serial No. 07/673,458, filed March 22, 1991, abandoned.
Prior application information: Examiner: J. Dudek Group/Art Unit: 2871

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label Customer No. 22204 or [X] Correspondence address below

(Insert Customer No. or Attach bar code label here)

Name Eric J. Robinson
Firm: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P C
Address 8180 Greensboro Drive, Suite 800
City. McLean State VA Zip Code 22102
Country· U.S A. Telephone (703) 790-9110 FAX (703) 883-0370

Name: Eric J. Robinson Registration No. 38,285

Signature Date: June 2, 1999

Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)	
Shunpei YAMAZAKI et al.	)	
Based On Serial No. 08/964,028	)	Art Unit: 2871
Which Was Filed: November 4, 1997	)	Examiner: J. Dudek
For: ELECTRO-OPTICAL DEVICE AND	)	
DRIVING METHOD FOR THE	)	
SAME	)	Date: June 2, 1999

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of application Serial No. 08/964,028, filed November 4, 1997; which itself is a Divisional of Serial No. 08/766,709, filed December 13, 1996, now U.S. Patent 5,905,555; which is a Divisional of Serial No. 08/542,821, filed October 13, 1995, now U.S. Patent 5,612,799; which is a Divisional of

Serial No. 08/224,992, filed April 8, 1994, now U.S. Patent 5,495,353; which is a Divisional of Serial No. 07/673,458, filed March 22, 1991, abandoned.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

TITLE OF THE INVENTION

ELECTRO-OPTICAL DEVICE AND DRIVING METHOD FOR THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a grey tone display and a driving method for the same and, more particularly to a display driving system utilizing complimentary thin film gate insulated field effect transistors suitable for used in liquid crystal displays.

2. Description of the Prior Art

There have been well known in the art active liquid crystal displays which are driven by thin film transistors (TFTs). The displays of this type comprise visual panels and peripheral circuits for driving the panel. The peripheral circuit is formed by attaching a single crystalline chip containing integrated circuits on a glass substrate by tab-bonding or COG (chip on glass). The visual panel comprises a plurality of pixels each being provided with a driving TFT. The TFT is usually an N-channel FET formed within an amorphous or polycrystalline semiconductor film which is electrically coupled to a respective pixel.

Fig.1 is a diagram illustrating the equivalent circuit of an exemplary liquid crystal display. The diagram shows only a 2 x 2 matrix for the sake of convenience in description whereas ordinary liquid crystal displays consist of more great numbers of pixels such as those in the form of a 640 x 480 matrix, a 1260 x 960 matrix and so on. The liquid crystal display includes a liquid crystal layer 42 disposed between a pair of glass substrates 11 and 11' as shown in Fig.2. Numeral 54 designates a polarizing plate. The inner surface of the glass substrate 11' is coated with a ground electrode 53. The inner surface of the other substrate 11 is provided with a plurality of conductive pads each constituting one pixel of the display. Each conductive pad are formed together with an n-channel FET 51 whose source is electrically connected with the corresponding pad. The drains of the FETs on a similar row in the matrix is connected with a control line of the row to

which control signals are supplied from a row driver 47. The gates of the n-channel FETs on a similar column are connected with a control line of the column to which control signals are supplied from a column driver 46.

In the operation of the display, the column driver 46 supplies control signals of a high level to selected columns to turn on the TFTs on the column. There are, however, undesirable cases in which the on-off action of the TFTs can not sufficiently carry out so that the output voltage of the TFT (i.e. the input to the pixel) reaches only short of a predetermined high voltage level (e.g. 5V), or the output voltage does not sufficiently fall to a predetermined low voltage (e.g. 0V). This is because of the asymmetrical characteristics of the TFTs. Namely, the charging action on the liquid crystal layer takes place in a dissimilar manner as the discharging action therefrom. Furthermore, since the liquid crystal is intrinsically insulating, the liquid crystal voltage (V_{LC}) becomes floating when the TFT is turned off. The amount of electric charge accumulated on the liquid crystal which is equivalent to a capacitance determines the V_{LC}. The accumulated charge, however, will leak through a channel resistance R_{SD} which may be formed by dust or ionized impurities or through the liquid crystal itself whose resistance R_{LC} 44 may be occasionally decreased. For this reason, V_{LC} sometimes becomes at an indeterminate intermediate voltage level. In the case of the panel having two hundred thousands to 5 million pixels, a high yield can not be expected in such a situation.

Also, in the conventional driving methods, the liquid crystal material to which control voltages are applied is subjected to an average electric field in one direction during operation. The electric field tends to cause electrolysis when continuously used. Because of this, the aging of the liquid crystal material is accelerated and the life time of the display is decreased.

Furthermore, it has been difficult to realize grey tone display, without complicated structure, capable of arbitrarily

displaying a variety of visual images in various shade of grey.

BRIEF SUMMARY OF THE INVENTION

It is an object of the present invention to provide a grey tone display and a driving method for the same capable of demonstrating clear visual images.

It is another object of the present invention to provide a grey tone display and a driving method for the same capable of accurate operation.

It is a further object of the present invention to provide a grey tone display and a driving method for the same capable of arbitrarily displaying a variety of visual images in various shade of grey.

Additional objects, advantages and novel features of the present invention will be set forth in the description which follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the present invention. The object and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

To achieve the foregoing and other object, and in accordance with the present invention, as embodied and broadly described herein, a display comprises a light influencing medium, electrode patterns defining a plurality of pixels in the medium and a control circuit for supplying control signals to the electrode patterns. The control circuit supplies the control signal to each pixel through a switching element which comprises at least one complimentary transistors connected between a low level and a high level. By the use of the conplimentary transistors, the voltage level of each pixel during its operation is prevented from fluctuating.

Particularly, the complimentary transistors are coupled in series at their source terminals to the output terminal of the complimentary transistors. The input terminal of the complimentary transistors is their gate terminals coupled to each other. By this

construction, when the complimentary transistors are connected between a suitable high voltage and a suitable low voltage, the output terminal of the complimentary transistors is brought to the input level at their gate terminals from which the threshold voltage is subtracted. Accodingly, the voltage applied to the light influencing voltage can be arbitrarily adjusted by regulating the input level resulting in visual images in various shade of grey. This is particularly fitted to light influencing mediums of dispersion type liquid crystals whose thresholds have certain widths.

In typical driving methods, the display of this type is driven by applying control signals in the form of pulses to conductive pads. The light influencing medium is disposed between the conductive pads and a back electrode. The back electrode is supplied with an alternate voltage in order to make zero the average voltage applied to the light influence medium.

In typical example, the present invention is applied to liquid crystal displays. Each pixel of the display is provided with a switching element of complimentary thin film field effect transistors which forcibly pull or push the level of the liquid crystal layer to a definite high or low voltage level rather than a floating state. Of course, the present invention can be practiced with a variety of other type transistors, other than thin film transistors, such as staggered types, coplanner types, inverted staggered types, inverted coplanner types. The channel regions of the transistors may be spoiled by introduction of a suitalbe impurity in order to eliminate the undesirable influence of incident light by reducing the photosensitivity of the transistors. When control transistors of a driver for supplying control signals to the switching transistors are formed also on the same substrate at its peripheral position where no light is incident, they are not spoiled by the impurity. In such a case, two types of transistors are formed on the substrate, one being spoiled and the other not being spoiled and having a carrier mobility 2 to 4 times larger than that of the spoiled transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the invention and, together with the description, serve to explain the principles of the invention.

Fig.1 is a schematic diagram showing an equivalent circuit of a liquid crystal display.

Fig.2 is a cross sectional schematic view showing an general configuration of a liquid crystal display.

Fig.3 is a schematic diagram showing an equivalent circuit of a liquid crystal display in accordance with a first embodiment of the present invention.

Figs.4(A), 4(B) and 4(C) are plan and cross sectional views showing the liquid crystal display illustrated in Fig.3.

Figs.5(A) and 5(B) are explanatory views demonstrating operation of the liquid crystal display in accordance with the first embodiment.

Fig.6 is a schematic view showing a system suitable for manufacturing thin film field effect semiconductor transistors in accordance with the present invention.

Fig.7(A) is a schematic view showing a planar type magnetron RF sputtering apparatus of the system illustrated in Fig.6 suitable for use in depositing oxide and semiconductor films.

Fig.7(B) is an explanatory view showing the arrangement of magnets provided in the apparatus as illustrated in Fig.7(A).

Figs.8(A) to 8(F) are cross sectional views showing a method of manufacturing thin film field effect semiconductor transistors suitable for the first embodiment of the present invention.

Fig.9(A) is a schematic diagram showing an equivalent circuit of a liquid crystal display in accordance with a second embodiment of the present invention.

Fig.9(B) is a plan sectional view showing the liquid crystal display illustrated in Fig.9(A).

Fig.10(A) is a schematic diagram showing an equivalent

circuit of a liquid crystal display in accordance with a third embodiment of the present invention.

Fig.10(B) is a plan sectional view showing the liquid crystal display illustrated in Fig.10(A).

Fig.11 is a schematic diagram showing an equivalent circuit of a liquid crystal display in accordance with a fourth embodiment of the present invention.

Fig.12 is an explanatory diagram demonstrating operation of the complimentary transistors of the liquid crystal display in accordance with the fourth embodiment.

Fig.13 is a chlonological diagram demonstrating operation of the liquid crystal display in accordance with the fourth embodiment.

Fig.14 is a schematic diagram showing an equivalent circuit of a liquid crystal display corresponding to Fig.13 in accordance with the fourth embodiment of the present invention.

Fig.15 is a schematic diagram showing an equivalent circuit of a liquid crystal display in accordance with a fifth embodiment of the present invention.

Fig.16 is a chlonological diagram demonstrating operation of the liquid crystal display in accordance with the fifth embodiment.

Fig.17 is a schematic diagram showing an equivalent circuit of a liquid crystal display in accordance with a sixth embodiment of the present invention.

Fig.18 is a chlonological diagram demonstrating operation of the liquid crystal display in accordance with the sixth embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig.3 is a diagram illustrating the equivalent circuit of a liquid crystal display in accordance with a first embodiment of the present invention. The diagram shows only a 2 x 2 matrix for the sake of convenience in description whereas ordinary liquid crystal displays consist of more great numbers of pixels such as a 640 x 480 matrix, a 1260 x 960 matrix. The liquid crystal display

includes a liquid crystal layer 42 disposed between a pair of glass substrates 11 and 11' as shown in Fig.2. The inner surface of the glass substrate 11' is coated with an electrode 53. The inner surface of the other substrate 11 is provided with a plurality of conductive pads 37b each constituting one pixel of the display as seen from Fig.4(A). Dashed line is enclosing one pixel in the figure. Each conductive pad 37b are formed on the substrate together with CMOS transistors consisting of an n-channel FET 51 and a p-channel FET 41 whose sources 34b' and 34b are electrically connected with the corresponding pad 37b. The drains of the n-channel FETs of the CMOSs on a similar row is connected with a V_{DD} line 48 of the row. The drains of the p-channel FETs of the CMOSs on a similar row is connected with a Vss line 49 of the row. The gates of the p-channel and n-channel FETs of the CMOSs on a similar column is connected with a V_{GG} line of the column. The Vss lines and the V_{DD} lines are connected with a row driver 47 and supplied with control signal therefrom. The V_{GG} lines 52 are connected with a column driver 46 and supplied with control signal therefrom. The column driver 46 and the row driver 47 are formed on the projected end of the glass substrate 11 as will be understood form the illustration of Fig.2.

When a TN liquid crystal material is used, the distance of the substrates is selected to be about 10 μm and both the inner surfaces of the substrates are provided with orientation control films which are given suitable rubbing treatment. When a ferroelectric liquid crystal (FLC) material is used, the distance of the substrates is selected to be about 1.5 to 3.5 μm, e.g. 2.3 μm and only one of the inner surfaces (the surface of the ground electrode) is provided with an orientation control film given suitable rubbing treatment. The driving voltage is ±20V. When a liquid crystal material of dispersion type or a polymer liquid crystal material is used, the distance of the substrates is selected to be about 1.0 to 10.0 μm, e.g. 2.3 μm and no orientation control film is necessary. The driving voltage is ±10 to ±15V. In this case, polarization plates are also unnecessary and therefore

the amount of available light can be relatively increased in either type of transmission and reflective types. Accordingly, whereas the liquid crystal layer possesses no threshold voltage, a large contrast in displayed images is realized and undesirable cross-talk is effectively prevented by the use of complimentary TFTs which provide a definite threshold voltage.

The operation of the complimentary transistors will be explained with reference to Figs.5(A) and 5(B). Let the V_{DD} line and the Vss line be in +10V and -10V respectively. The n-channel transistor 51 is tuned on and the p-channel transistor 41 turned off when a positive voltage V_{GG} is applied to the gate terminals 40 and 40' as illustrated in Fig.5(A). This condition continues until the source voltage level reaches V_{GG}-Vth. Namely, the n-channel transistor is turned off when the effective gate voltage (the gate voltage relative to the source voltage) comes short of the threshold voltage Vth. Of course, the n-channel transistor always supplies electric charge to the source terminal in order to maintain the source voltage level at that level coping with current leakage from the source terminal. Accordingly, the source terminal, i.e. the output level of the complimentary transistors is fixed to the V_{GG}-Vth level so that the output level can be controlled by the input gate signal.

Contrary to this, the n-channel transistor 51 is tuned off and the p-channel transistor 41 turned on when a negative voltage V_{GG} is applied to the gate terminals 40 and 40' as illustrated in Fig.5(B). This condition continues until the source voltage level falls to V_{GG}-Vth. Namely, the p-channel transistor is turned off when the effective gate voltage (the gate voltage relative to the source voltage) comes beyond the threshold voltage -Vth. Of course, the n-channel transistor always discharges the source terminal in order to maintain the source voltage level at that level coping with current leakage from the source terminal. Accordingly, the source terminal, i.e. the output level of the complimentary transistors is fixed to the V_{GG}-Vth level so that the output level can be controlled by the input gate signal also

in this case.

Referring now to Fig.6, Figs.7(A) and 7(B) and Figs.8(A) to 8(F), a method of manufacturing gate insulated field effect transistors 41 and 51 constituting a CMOS in accordance with a first embodiment of the present invention will be explained. Fig.6 is a schematic view showing multi-chamber sputtering system for depositing semiconductor and oxide films by magnetron RF sputtering. The system comprises a loading and unloading pre-chamber 1 provided with a gate valve 5, a subsidiary chamber 2 connected to the pre-chamber 1 through a valve 6 and first and second individual sputtering apparatuses 3 and 4 connected to the subsidiary chamber 2 respectively through valves 7 and 8. The pre-chamber 1 is provided with an evacuation system 9 comprising a rotary pump and a turbo molecular pump in series. The subsidiary chamber 2 is provided with a first evacuation system 10a for roughing comprising a rotary pump and a turbo molecular pump in series, a second evacuation system 10b for high vacuum evacuation comprising a cryosorption pump and a heater 10c located in the chamber 2 in order to heat substrates to be coated. If substrates to be coated are thermally contracted in advance by heating in the subsidiary chamber 2, thermal contraction and stress caused in films during deposition thereof on the substrate is reduced so that the adhesivity of the films can be improved.

The sputtering apparatuses 3 and 4 are individual planar type magnetron RF sputtering apparatuses suitable for exclusive use in depositing oxide films and semiconductor films respectively when used in accordance with the present invention. Figs.7(A) and 7(B) illustrate details of the RF sputtering apparatus. The apparatus comprises a vacuum chamber 20, a first evacuation system 12-1 for roughing consisting of a turbo molecular pump 12b and a rotary pump 12d respectively provided with valves 12a and 12c, a second evacuation system 12-2 for high vacuum evacuation comprising a cryosorption pump 12e provided with a valve 12f, a metallic holder 13 fixed in the lower side of the chamber 20 for

supporting a target 14 thereon, formed with an inner conduit 13a through which a coolant can flow to cool the target 14 and provided with a number of magnets 13b such as parmanent magnets, an energy supply 15 consisting of an RF (e.g. 13.56MHz) source 15a provided with a matching box 15b for supplying RF energy to the holder 13, a substrate holder 16 located in the upper position of the chamber 20 for supporting a substrate 11 to be coated, a heater 16a embedded in the substrate holder 16, a shutter 17 intervening the substrate 11 and the target 14 and a gas feeding system 18. Numeral 19 designates sealing means for ensuring air-tight structure of the vacuum chamber 20. In advance of actual deposition on the substrate 11, impurities occurring in the targets are sputtered and deposited on the shutter 17 intervening the substrate 11 and the target 14, and then the shutter is removed in order to enable normal deposition on the substrate 11. The magnets 13b are oriented to have their N poles at the upper ends and S poles at the lower ends and horizontally arranged in a circle as illustrated in Fig.7(B) in order to confine electrons in a sputtering region between the substrate 11 and the target 14.

Referring now to Figs.8(A) to 8(F) together with Fig.6 and Figs.7(A) and 7(B), a method of manufacturing thin film field effect transistors 41 and 51 in accordance with the first preferred embodiment of the invention will be described in details. This exemplary method is carried out with a multi-chamber apparatus suitable for mass-production. This is, however, applicable to similar processes utilizing separate chambers without substantial modification.

10 sheets of glass substrate are mounted on a cassette and placed in the loading and unloading pre-chamber 1 through the valve 5. The substrates may be made from an inexpensive glass which can endure thermal treatment at high temperatures up to 700℃, e.g. about, 600℃ such as NO glass manufactured by Nippon Electric Glass Co. Ltd., LE-30 glass manufactured by Hoya Co. or VYCOR glass manufactured by Corning Corp. After adjusting the inner conditions of the pre-chamber 1 and the subsidiary chamber 2

to each other, the cassette is transported from the pre-chamber 1 into the subsidiary chamber 2 through the valve 6. One of the glass substrates is disposed in the first magnetron RF sputtering apparatus as shown in Fig.7(A) by means of a transportation mechanism (not shown) and coated with a SiO_2 film 32 as a blocking film to a thickness of 1000Å to 3000Å in a 100% O_2 atmosphere (0.5 Pa) at a substrate temperature of 150℃. The output power of the apparatus is 400W to 800W in terms of 13.56 MHz RF energy. A single crystalline silicon or a quartz block is used as a target. The deposition speed is 30 to 100 Å/min. The coated substrate is then exchanged by another of the remaining 9 substrate which is subsequently coated with a SiO_2 film in the same manner. All the substrates mounted on the cassette are coated with a SiO_2 film by repeating this procedure. During this procedure, the transportation of a substrate between the pre-chamber 1 and the subsidiary chamber 2 has to be carried out after adjusting the pressures and the inner atmospheres of the chambers 1 and 2 to each other in order to eliminate undesirable impurities.

An amorphous silicon film 33 is next deposited in the second sputtering apparatus 4 on the SiO_2 film 32 to a thickness of 500 nm to 1 μm, e.g. 2000Å. The total density of oxygen, carbon and nitrogen in the amorphous film is preferably between 5×10^{20} to 5×10^{21} cm^{-3} in order to eliminate undesirable influence of incident light on the channel region of the transistor by reducing photosensitivity. The photosensitivity of the channel can be alternatively reduced by introducing an spoiling impurity selectively into the channel. In this case, the total density of oxygen, carbon and nitrogen in the amorphous film does desirably not exceed 7×10^{20} cm^{-3}, preferably not to exceed 1×10^{19} cm^{-3}. Such low density makes it easy to recrystallize the source and the drain to be formed in the silicon film in the latter step by thermal treatment. For the formation of the silicon film 33, the 10 substrates are placed into the apparatus 4 one after another from the subsidiary chamber 2 in the same manner and treated therein for deposition of the amorphous silicon film. The

transportation of each substrate between the apparatus 4 and the subsidiary chamber 2 is carried out after adjusting the pressures and the inner atmospheres of the chambers 2 and 4 in order to eliminate undesirable impurities. This procedure is generally employed when it is desired to transport the substrates between the first or second sputtering apparatus and the subsidiary chamber, even if not particularly described hereinbelow. The atmosphere in the apparatus 4 comprises a mixture consisting of hydrogen and argon so that $H_2/(H_2+Ar) = 0.8$ (0.2 to 0.8 in general) in terms of partial pressure. The hydrogen and argon gases have desirably purities of 99.999% and 99.99% respectively and are introduced after the inside of the apparatus 4 is evacuated to a pressure not higher than 1×10^{-5} Pa. The total pressure is 0.5 Pa: the output power of the apparatus is 400W to 800W in terms of 13.56 MHz RF energy: a single crystalline silicon desirably containing oxygen atoms at a concentration of no higher than $5 \times 10^{18} cm^{-3}$, e.g. $1 \times 10^{18} cm^{-3}$ is used as a target: and the substrate temperature is maintained at 150℃ (deposition temperature) by the heater 16a in the same manner. In preferred embodiments, the hydrogen proportion in the mixture may be chosen between 5% and 100%; the deposition temperature between 50℃ and 500℃, e.g. 150℃; the output power between 1W and 10MW in a frequency range from 500Hz to 100GHz which may be combined with another pulse energy source.

Alternatively, the amorphous silicon film 33 may be deposited by low pressure CVD (LPCVD) or plasma CVD. In the case of LPCVD, the deposition is carried out by introducing disilane (Si_2H_6) or trisilane (Si_3H_8) in a suitable CVD chamber. The deposition temperature is selected at a temperature 100℃ to 200℃ lower than the recrystallization temperature of the silicon, i.e. 450℃ to 550℃, for example 530℃. The deposition speed is 50 to 200Å/min. Boron may be introduced at $1 \times 10^{15} cm^{-3}$ to $1 \times 10^{16} cm^{-3}$ into the film by using diboran as a dopant gas together with the silane in order to make even the threshold voltages of N-type and P-type TFTs. In the case of plasma CVD, the deposition is carried

out by introducing monosilane (SiH_4) or disilane (Si_2H_6) at 300℃ in a suitable plasma CVD chamber. The input energy is for example high frequency electric energy at 13.56MHz.

The oxygen density of the semiconductor film are preferably no higher than 5 x $10^{21}cm^{-3}$ because if the oxygen density is too high, thermal treatment have to be carried out at a high temperature for a long time in order to sufficienty recrystallize the semiconductor film in a latter step. The oxygen density, however, must not be too low because leak current in the off condition of the TFT increases in response to a back light which may be provided in the liquid crystal display if particular spoiling impurity is not used. For this reason, the oxygen density is selected between 4 x 10^{19} to 4 x $10^{21}cm^{-3}$. In accordance with experiments, it was confirmed by SIMS (secondary ion mass spectroscopy analysis) that hydrogen was involved at densities of 4 x $10^{20}cm^{-3}$ equivalent to one atom % assuming the density of silicon being 4 x $10^{22}cm^{-3}$. These figures of density were minimum values of the respective elements which varied along the depth direction. The reason why such minimum values were employed is that a natural oxide existed at the surface of the semiconductor film. If it is desired to spoil the channel regioin, oxygen may be introduced as a spoiling agent to a portion of the semiconductor film to be a channel region to a density of 5 x 10^{20} to 5 x $10^{21}cm^{-3}$ after deposition of the semiconductor film. In this case, the deposition of the semiconductor film can be carried out in order that the total density of oxygen in the semiconductor film does not exceed 7 x $10^{20}cm^{-3}$, preferably not to exceed 1 x $10^{19}cm^{-3}$. Such low density makes it easy to recrystallize the source and drain regions of the semiconductor film in the latter step by thermal treatment. In this case, when TFTs for peripheral circuits located not to be exposed to illumination are formed in the same time, the mobility of the TFTs can be increased, because the oxygen introduction is prevented, resulting in a high speed operation.

After all the substrates are coated with the silicon oxide and amorphous silicon semiconductor films, thermal treatment

is given thereto in the subsidiary chamber 2 by means of the heater 10c at 450℃ to 700℃, typically at 600℃ for 12 to 70 hours in a non-oxidizing atmosphere, e.g. in hydrogen. The film is recrystallized by this treatment (thermal annealing) in the form of semi-amorphous or semi-crystalline structure.

Next, the mechanism of formation of semi-amorphous or semi-crystalline semiconductor material in accordance with the present invention will be explained. When sputtering a single crystalline silicon target in a mixture of hydrogen and argon, high energy heavy argon atoms collide with the surface of the target, dislodge therefrom clusters each consisting of several tens to several hundred thousands of silicon atoms, and deposit the clusters on a substrate to be coated. These clusters pass through the mixture gas in advance of the deposition on the substrate and are coupled with hydrogen atoms at their external surfaces in order to terminate their dangling bonds. Accordingly, when deposited on the substrate, the clusters comprise internal amorphous silicon and external ordered silicon including Si-H bonds. The Si-H bonds react with other Si-H bonds and are converted to Si-Si bonds by thermal treatment at 450℃ to 700℃ in a non-oxidizing atmosphere. These coupling of adjacent silicon atoms (Si-Si) function to let adjacent clusters be attracted to each other whereas these clusters have a tendency to convert their phases to more ordered phases (partial recrystallization). As a result, the crystalline structure of these clusters is given lattice distortion and the peak of its Raman spectra ($522cm^{-1}$: the peak of single crystalline silicon) is displaced to the low frequency direction. The apparent grain diameter calculated based on the half-width is 50 to 500Å which seems to indicate microcrystals.

The energy bands of the clusters are connected through the Si-Si bonds anchoring the clusters at the interfaces therebetween. For this reason, the polycrystalline (semi-amorphous or semi-crystalline) structure of silicon in accordance with the present invention is entirely different than usual polycrystals in

which grain boundaries provide barriers against carrier transportation, so that the carrier mobility can be on the order of 15 to 300 $cm^2/Vsec$ (electron mobility) and 10 to 200 $cm^2/Vsec$ (hole mobility). Namely, the semi-amorphous or semi-crystalline structure in accordance with the present invention can be considered substantially not to include undesirable grain boundaries. Of course, if the semiconductor is subjected to high temperatures of 1000℃ or higher rather than the relatively low temperatures of 450℃ to 700℃, latent oxygen atoms come to appear at the boundaries between the clusters and form barriers like the prior art technique. The carrier mobility can be improved by increasing the strength of the anchoring. For this purpose, the oxygen density in the semiconductor film is decreased to $7 \times 10^{19} cm^{-3}$, desirably to $1 \times 10^{19} cm^{-3}$.

The amorphous silicon semiconductor film 33 is patterned by means of a photomask as indicated by (I) to leave areas 33 and 33' which are necessary to form N-channel and P-channel transistors. After all the substrates are coated with the silicon oxide and amorphous silicon semiconductor films and patterned as described above, the substrates are placed again in the first sputtering apparatus 3. The entire structure is then coated with a silicon oxide film 35 of a thickness of 500Å to 2000Å, e.g. 1000Å by sputtering in an oxide atmosphere as illustrated in Fig.8(B). The deposition condition is same as that of the silicon oxide film 32 explained above. The characteristics at the interface between the silicon oxide film 35 and the underlying semiconductor film 33 can be improved by applying ultraviolet rays to carry out ozone oxidation. Namely, the interface states can be decreased by utilizing photo-CVD in combination with the sputtering explained in the description of deposition of the oxide film 32. Alternatively, fluorine may be introduced in this deposition in order to fix sodium ions. In this case, the atmosphere comprises a high density oxygen (95%) including NF_3 (5%) at a total pressure of 0.5 Pa: the output power of the apparatus is 400W in terms of 13.56 MHz RF energy: a single crystalline silicon or an artificial

quartz is used as a target: and the substrate temperature is maintained at 100℃. By this procedure, the silicon oxide film 35 to be a gate insulating film includes fluorine atoms which function to terminate dangling bonds of silicon atoms so that the formation of fixed charge can be prevented at the interface between the semiconductor films 33 and 33' and the oxide film 35. On the silicon oxide film 35 is deposited by low pressure CVD a silicon semiconductor film of 0.2 μm thickness which is highly doped with phosphorus at 1×10^{21} to $5 \times 10^{21} cm^{-3}$ followed, if desired, by coating a conductive film of 0.3 μm thickness made of molybdenum, tungsten film or a multiple film consisting of it and a $MoSi_2$ or WSi_2 film. The semiconductor film coated with the conductive (multiple) film is then patterned by photolithography with a suitable mask ② in order to form gate electrodes 40 and 40'.

A photoresist film 27' is formed by the use of a photomask ③ in order to cover the semiconductor film 33'. With the gate electrode 40 and the photoresist film 27', self-aligned impurity regions, i.e. a source and a drain region 34a and 34b are formed by ion implantation of boron at $1 \times 10^{15} cm^{-2}$ to $5 \times 10^{15} cm^{-2}$. The intermediate region 28 of the silicon semiconductor film 33 between the impurity regions 34a and 34b is then defined as a channel region as illustrated in Fig.8(C). After removing the photoresist film 27', another photoresist film 27 is formed by the use of a photomask ④ in order to cover the semiconductor film 33. With the gate electrode 40' and the photoresist film 27', self-aligned impurity regions, i.e. a source and a drain region 34b' and 34a' are formed by ion implantation of phosphorus at $1 \times 10^{15} cm^{-2}$ to $5 \times 10^{15} cm^{-2}$. The intermediate region 28' of the silicon semiconductor film 33 between the impurity regions 34a' and 34b' is then defined as a channel region as illustrated in Fig.8(D). The channel lengths of the p-channel and n-channel transistor are 10 μm respectively. The channel widths of the p-channel and n-channel transistor are 20 μm respectively. The ion implantation may instead be carried out by selectively removing

the silicon oxide film 35 by the use of the gate electrode 40 or 40' as a mask followed by direct ion implantation of boron or phosphorus.

After removing photoresist 27, the channel regions are then thermally annealed at 600℃ for 10 to 50 hours in H_2 atmosphere to make active the impurities in the drain and source regions. An interlayer insulating film 37 of silicon oxide is deposited to a thickness of 0.2 to 0.6 μm by the same sputtering method as described above over the entire surface of the structure followed by etching by means of a photomask ⑤ for opening contact holes 39 through the interlayer film 37 and the oxide film 35 in order to provide accesses to the underlying source and drain regions 34b, 34a, 34b' and 34a'. The deposition of the interlayer insulating film 37 may be carried out by LPCVD, photo-CVD, ordinal pressure CVD(TEOS-ozone). Next, an aluminum film of 0.5 to 1 μm thickness is deposited on the structure over the contact holes 39 and patterned to form source and drain electrodes 36b, 36a, 36b' and 36a' by means of a photomask ⑥ as illustrated in Fig.8(F). An organic resin film 39 such as a transparent polyimide film is coated over the structure to provide a planar surface and patterned by means of a photomask ⑦ to provide accesses to the source electrodes 36b and 36b' followed by formation of lead electrode 37 made of a transparent conductive material such as indium tin oxide (ITO) to be electrically connected with the pad 37b. The ITO film is deposited by sputtering at room temperature to 150℃ followed by annealing in an oxidizing atmosphere (O_2) or in air at 200 to 400℃. The pad 37b can be formed at the same time by the deposition of the lead electrode 37. Then, the formation of CMOS transistors is finished. The mobility, the threshold voltage of the p-channel TFT are 20 cm^2/Vs and -5.9 V. The mobility, the threshold voltage of the n-channel TFT are 40 cm^2/Vs and 5.0 V. The glass substrate thus provided with these CMOS transistors and suitable conductive patterns as illustrated is joined with a counterpart glass substrate provided with a ground electrode at its entire inner surface followed by injection of a liquid crystal

material between the two substrates. One of the advantages of the above process is that the formation of these transistors (spoiled and not spoiled) can be carried out at temperatures no higher than 700℃ so that the process does not require the use of expensive substrates such as quartz substrates and therefore suitable for large scale liquid crystal displays production methods.

In the above embodiment, thermal annealing is carried out twice at the steps corresponding to Figs.8(A) and 8(D). The first annealing (Fig.8(A)), however, can be omitted to shorten the process time in the light of the second annealing.

Referring to Figs.9(A) and 9(B), CMOS thin film field effect transistors in accordance with a second preferred embodiment of the present invention will be illustrated. In this embodiment, two couples of CMOS transistors 51-1, 41-1, 51-2 and 51-2 are connected in parallel to the conductive pad 37b for each pixel (as enclosed by dashed line) at their source electrodes. These CMOS transistors are manufactured in the steps explained above in conjunction with the first embodiment except that the number of the transistors is doubled. The similar elements are given similar numerals as in the first embodiment. The electrode pads 37b have to be deposited on the V_{GG} line through a suitable insulating film therebetween. The electrical operation is substantially same as that of the first embodiment. Accordingly, two identical individual switching elements are prepared corresponding to one pixel so that when the operation of one of them is fault, the ability of information display can be maintained by firing the fault element by laser rays in virtue of the remaining CMOS transistors. For this reason, the conductive transparent pads are formed in order not to cover these TFTs.

Referring to Figs.10(A) and 10(B), CMOS thin film field effect transistors in accordance with a third preferred embodiment of the present invention will be illustrated. Also in this embodiment, two couples of CMOS transistors 51-1, 41-1 and 51-2 and 41-2 are connected in parallel to an electrode pad 37b for each pixel at their source electrodes. The electrode pad 37b,

however, is separated into two portions 37b-1 and 37b-2 each independently connected to a corresponding one of the two CMOS transistors. These CMOS transistors are manufactured in the steps explained above in conjunction with the first embodiment except for the number of the transistors. The similar elements are given similar numerals as in the first embodiment. Then, each pixel comprises two individual sub-pixels. In accordance with this embodiment, even if the operation of one of the sub-pixels is fault, the other sub-pixel can support the operation of the pixel and therefore the deterioration of grey scales is substantially decreased.

As described above, there are following advantages in accordance with the above embodiments of the present invention:

1) Visual images can be constructed in a variety of grey shade.

2) The voltage across the liquid crystal layer is stably fixed at determinate level in accordance with the output signal from the complimentary transistors rather than in an indeterminate floating condition.

3) Margins for operational fluctuation are broadened.

4) Even if some TFTs are fault, the operation thereof is followed up to same extent.

5) The increase of the number of photomasks due to the employment of complimentary transistors is only two (photomask ③ and ④) as compared with conventional cases utilizing only n-channel TFTs.

6) Since semi-amorphous or semi-crystalline semiconductors are used in place of amorphous semiconductors and the carrier mobility is increased by a factor of ten or more, the size of the TFT is substantially reduced so that little decrease of the aperture ratio is necessary even when two TFTs are formed in one pixel.

Fig.11 is a diagram illustrating the equivalent circuit of a liquid crystal display in accordance with a fourth embodiment of the present invention. The pixel configuration as shown in

Fig.4 can be applied also for this embodiment. The diagram shows only a 2 x 2 matrix for the sake of convenience in description whereas ordinary liquid crystal displays consist of more great numbers of pixels such as a 640 x 480 matrix, a 1260 x 960 matrix. The liquid crystal display includes a liquid crystal layer 42 disposed between a pair of glass substrates 11 and 11' in the same manner as the first embodiment as shown in Fig.2. The entirety of the inner surface of the glass substrate 11' is coated with a back electrode 53. In this embodiment, however, the electrode 53 is not ground but supplied with an offset voltage in accordance with the driving mechanism of the liquid crystal display as detailedly explained infra. The inner surface of the other substrate 11 is provided with a plurality of conductive pads 37b each constituting one pixel of the display in the same manner as the first embodiment. Each conductive pad 37b are formed on the substrate together with CMOS transistors consisting of an N-type FET 51 and a P-type FET 41 whose sources 34b' and 34b are electrically connected with the corresponding pad 37b. The drains of the N-type FETs of the CMOSs on a similar row are connected with a V_{DD} line 48 of the row. The drains of the P-type FETs of the CMOSs on a similar row is connected with a Vss line 49 of the row. The gates of the P-type and N-type FETs of the CMOSs on a similar column is connected with a V_{GG} line of the column. The Vss lines and the V_{DD} lines are connected with a row driver 47 and supplied with control signal therefrom. The V_{GG} lines 52 are connected with a column driver 46 and supplied with control signal therefrom.

Fig.12 illustrates operational action of each pixel in response to several control signals applied to the V_{DD} line, the V_{SS} line, the V_{GG} line and the back electrode. When a positive voltage is applied to the V_{DD} line and a negative voltage to the V_{SS} line, the liquid crystal voltage level at the pixel (i.e. the voltage level of the pad 37b) follows the voltage level at the V_{GG} line and the liquid crystal voltage level is forcibly at ground if the V_{DD} line and the Vss line are commonly grounded. Accordingly, the voltage applied between the liquid crystal at the pixel is

calculated by subtracting the offset (bias) voltage applied to the back electrode from the liquid crystal voltage.

The representative example of the driving method in accordance with the fourth embodiment of the present invention will be explained with reference to Figs.13 and 14. In Fig.14, the 2 x 2 matrix of Fig.11 is expanded to a 4 x 4 matrix. The configurations of them, however, are substantially indentical except the number of pixels. Fig.13 illustrates the control signals applied to the V_{DD} lines, the V_{SS} lines, the V_{GG} lines and the back electrode. The V_{DD} lines are called X_{1a}, X_{2a}, X_{3a} and X_{4a} from the first row to the forth row in the diagram whereas the Vss lines are called X_{1b}, X_{2b}, X_{3b} and X_{4b} in the same manner. The signals applied to the Vss lines are exactly the inversion of the signals to the V_{DD} line and therefore the waveforms of the Vss lines are dispensed with in the illustration. The V_{GG} lines are called Y_1, Y_2, Y_3 and Y_4 from the left column to the right column. In this driving method, the control signals applied to the V_{DD} and Vss lines are addressing signals which scan from the first row to the forth row as shown in Fig.13. Opposed pulses are applied to the V_{DD} and Vss lines connected to one addressed row for the time width of one fourth of the frame during which all the rows are sequentially scanned. The control signals applied to the V_{GG} lines are data signals which determine the visual pattern appearing on the display.

If a pixel on the i-th row and the j-th column is desired to be actuated, a positive pulse is applied to the V_{GG} line of the j-th column at the time when the i-th row is addressed by applying opposed pulses to the VDD and Vss lines on the i-th row. In Fig.13, the pixel on the first column and the first row (given symbol AA in Fig.14) is actuated in the first fourth of the first frame between T_1 and T_2, the second frame between T_2 and T_3 and the fifth frame between T_5 and T_6. The back electrode is biassed by a negative voltage between T_1 and T_6. The V_{DD}, Vss and V_{GG} signal levels and the bias voltage are for example 20V, -20V, +20V and +10V respectively in the case that the optical

characteristic of the liquid crystal is changed by the threshold voltage of 20V thereacross. Accordingly, as understood from Fig.12, such a high voltage as 30V is applied only to the selected pixel (the AA pixel in the figure) while the voltage level applied to the other pixel can not exceed 10V. In T_6 to T_8 in Fig.13, the voltage levels at the V_{GG} lines and the back electrode are inversed so that the sign of the applied voltage on each pixel is simply inversed. Accordingly, such a low voltage as -30V is applied only to the selected pixel (the AA pixel in the figure) while the absolute voltage level applied to the other pixel can not exceed 10V. The pixel on the first column and the first row is actuated in the sixth frame between T_6 and T_7. The inversion of the signs takes place repeatedly once per several frames to several tens of frames so that the average voltage applied to the liquid crystal approaches to zero throughout the operation resulting in effective prevention of deterioration of the liquid crystal.

In accordance with this embodiment, the voltage level of control signals applied to the liquid crystal layer can be easily adjusted to the threshold level of the liquid crystal layer only by adjusting the bias voltage level applied to the back electrode. The employment of the bias voltage makes it possible to cancel out the effect of the electric field impressed on the liquid crystal by periodically chaning the polarity of the bias voltage, resulting in the prevention of electrolysis of the liquid crystal material.

Referring to Figs.15 and 16, a liquid crystal display and a method for driving the display in accordance with a fifth preferred embodiment of the present invention will be illustrated. In this embodiment, two couples of CMOS transistors 41-1, 51-1 and 41-2', 51-2' are connected in parallel to an electrode pad 33 for each pixel (as enclosed by dashed line) at their source electrodes. These CMOS transistors are manufactured in the steps explained above in conjunction with the first embodiment except that the number of the transistors is doubled. The similar

elements are given similar numerals as in the first embodiment. The electrical operation is substantially same as that of the third embodiment. Accordingly, two identical individual switching elements are prepared corresponding to one pixel so that when the operation of one of them is fault, the ability of information display can be maintained by firing the fault element by laser rays in virtue of the remaining CMOS transistors. For this reason, the conductive transparent pads are formed in order not to cover these TFTs.

The representative example of the driving method in accordance with the third embodiment of the present invention will be explained with reference to Fig.16. In Fig.16, explanation is made for the display as shown in Fig.15 but expanded in a 4 x 4 matrix. The configuration, however, is substantially indentical except the number of pixels. Fig.16 illustrates the control signals applied to the V_{DD} lines, the V_{SS} lines, the V_{GG} lines and the back electrode in the same manner as the second embodiment. In this driving method, the control signals applied to the V_{GG} lines are addressing signals which repeatedly scan from the first row to the fourth row as shown in Fig.16. A negative or positive pulse is applied to the V_{GG} line connected to an addressed column. The control opposite signals applied to the V_{DD} and Vss lines are data signals which determine the visual pattern appearing on the display.

If a pixel on the i-th row and the j-th column is desired to be actuated, opposed pulses are applied to the V_{DD} and Vss lines of the i-th row at the time when the j-th column is addressed by applying a positive pulse to the V_{GG} line on the j-th column. In Fig.16, the pixel on the first column and the first row is actuated in the first frame between T_1 and T_2, the second frame between T_2 and T_3 and the fifth frame between T_5 and T_6. The back electrode is biassed by a negative voltage between T_1 and T_6. The V_{DD}, Vss and V_{GG} signal levels and the bias voltage are for example 20V, -20V, +20V and +10V respectively in the case that the optical characteristic of the liquid crystal is changed by the

threshold voltage of 20V. Accordingly, as understood from Fig.12, such a high voltage as 30V is applied only to the selected pixel while the voltage level applied to the other pixel can not exceed 10V. In T_0 to T_8 in Fig.16, the voltage levels at the V_{GG} lines and the back electrode are inversed so that the sign of the applied voltage on each pixel is simply inversed. Accordingly, such a low voltage as -30V is applied only to the selected pixel while the absolute voltage level applied to the other pixel can not exceed 10V. The pixel on the first column and the first row is actuated in the sixth frame between T_6 and T_7. The inversion of the signs takes place repeatedly once per several frames to several tens of frames so that the average voltage applied to the liquid crystal approaches to zero resulting in effective prevention of deterioration of the liquid crystal.

Referring to Figs.17 and 18, a sixth preferred embodiment of the present invention will be illustrated. Also in this embodiment, two couples of CMOS transistors 41-1, 51-1 and 41-2', 51-2' are connected in parallel to an electrode pad 37b for each pixel at their source electrodes. The electrode pad 37b, however, is separated into two portions 37b-1 and 37b-2 each independently connected to a corresponding one of the two CMOS transistors in the same manner as Fig.10(B). These CMOS transistors are manufactured in the steps explained above in conjunction with the first embodiment except for the number of the transistors. The similar elements are given similar numerals as in the first embodiment. Then, each pixel comprises two individual sub-pixels. In accordance with this embodiment, even if the operation of one of the sub-pixels is fault, the other sub-pixel can support the operation of the pixel and therefore the possibility of deterioration in grey scale is substantially decreased. Also, even when the operational speed of one sub-pixel becomes low, the quality of the displayed image is not so deteriorated.

The representative example of the driving method in accordance with the sixth embodiment of the present invention will

be explained with reference to Fig.18. In Fig.18, explanation is made for the display as shown in Fig.17 but expanded in a 4 x 4 matrix. The configuration, however, is substantially indentical except the number of pixels. Fig.18 illustrates the control signals applied to the V_{DD} lines, the V_{SS} lines, the V_{GG} lines and the back electrode in the same manner as the fourth embodiment. In this driving method, the control signals applied to the V_{DD} and Vss lines are addressing signals which scan from the first row to the forth row as shown in Fig.18. Opposed pulses are applied to the V_{DD} and Vss lines connected to an addressed row. The control signals applied to the V_{GG} lines are data signals which determine the visual pattern appearing on the display. In this embodiment, however, control signals applied to the V_{GG} lines are positive or negative pulses whose pulse width is only one 16th of one frame (e.g. between T_1 and T_2). The pulse width of addressing signals applied to the V_{DD} and Vss lines is on the other hand one fourth of the frame in the same manner as the second embodiment. The 16th division fashion is suitable for color displays.

If a pixel on the i-th row and the j-th column is desired to be actuated, a positive pulse is applied to the V_{GG} line of the j-th column at the time when the i-th row is addressed by applying opposed pulses to the VDD and Vss lines on the i-th row. In Fig.18, the pixel on the first column and the first row is actuated in the first frame between T_1 and T_2. The back electrode is biassed by a negative voltage between T_1 and T_3. The V_{DD}, Vss and V_{GG} signal levels and the bias voltage are for example 20V, -20V, +20V and +10V respectively in the case that the optical characteristic of the liquid crystal is changed by the threshold voltage of 20V in the same manner. Accordingly, as understood from Fig.18, such a high voltage as 30V is applied only to the selected pixel while the voltage level applied to the other pixel can not exceed 10V. In T_3 to T_4 in Fig.18, the voltage levels at the V_{GG} lines and the back electrode are inversed so that the sign of the applied voltage on each pixel is simply inversed. Accordingly, such a low voltage as -30V is applied only to the selected pixel

while the absolute voltage level applied to the other pixel can not exceed 10V. The pixel on the first column and the first row is actuated in the third frame between T_3 and T_4. The inversion of the signs takes place repeatedly once per several frames to several tens of frames so that the average voltage applied to the liquid crystal approaches to zero resulting in effective prevention of deterioration of the liquid crystal.

The foregoing description of preferred embodiments has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and obviously many modifications and variations are possible in light of the above teaching. The embodiment was chosen in order to explain most clearly the principles of the invention and its practical application thereby to enable others in the art to utilize most effectively the invention in various embodiments and with various modifications as are suited to the particular use contemplated. Examples are as follows:

The above embodiments are applications in the form of CMOSs for switching devices in liquid crystal displays. The TFT in accordance with the present invention, however, can be utilized in the form of a switching device comprising one TFT for driving one pixel. In this case, the equivalent circuit is substantially same as that illustrated in Fig.1 except that the resister R_{SD} is not effective because the N-type TFT is constructed with a spoiled semiconductor film which is not sensitive to incident light as explained above. The electrode pad of each pixel becomes electrically floating when not addressed in this modification so that the voltage level thereof may not be so fixed as compared with those utilizing CMOSs. The manufacturing process thereof, however, is very simple without the need of light blocking means.

The liquid crystal material used in the liquid crystal display may include other type materials. For example, a suitable phase transition liquid crystal materials can be prepared by adding an ion dopant into a nematic liquid crystal material of

guest-host type or dielectric anisotropic type. The phase transition liquid crystal material changes, in accordance with application of an electric field, its optical appearance from a transparent state to a cloudy state and vice versa through phase transition between its nematic phase and its cholesteric phase. Furthermore in place of liquid crystals, suitable light influencing materials are also utilized in the same purpose such as electrophoresis dispersions which are prepared by dispersing pigment particles in an organic liquid which has been colored by a dye. If grey scale is desired, a plurality of frames are given to one image to be displayed and selected pixels are actuated only in a fewer frames than the given frames in accordance with the desired grey tone.

The present invention can be applied to displays utilizing other types of semiconductor devices such as germanium or silicon/germanium (Si_xGe_{1-x}) semiconductor devices, in which case the thermal treatment can be done at temperatures approx. 100℃ lower than those used for silicon semiconductors in the above embodiments. The deposition of such semiconductor can be carried out by sputtering in a high energy hydrogen plasma caused by optical energy (shorter than 1000 nm wavelength) or electron cyclotron resonance (ECR). Instead of gases including hydrogen molecules, some hydrogen compounds can be used as the atmosphere of sputtering as long as not to be impurity. For example, monosilane or disilane may be used for forming silicon semiconductor transistors. Although in the preferred embodiments, oxide and semiconductor films are deposited respectively in separate apparatuses, it is apparently also possible to deposit other types of gate insulating films or gate electrodes in a common apparatus. During deposition of oxide films, a halogen such as fluorine may be used as an atmosphere of sputtering so as to introduce halogen atoms into the oxide films in order to effectively prevent alkali metal atoms from getting into the film from the glass substrate by virtue of neutralization. The same effect can be expected by introduction of phosphorus in place of

halogens.

The present invention can be applied for other types of optical devices utilizing semiconductor devices such as image sensors, load elements or three-dimensional elements of monolithic integrated semiconductor devices. In the preferred embodiments field effect transistors are formed on a glass substrate. However, other substrates can be used instead. For example, thin film field effect transistors may be formed on a silicon substrate in a liquid crystal display or an image sensor device. This silicon substrate may be an intrinsic silicon substrate, a p-type silicon substrate, an n-type silicon substrate, or a silicon substrate in which MOSFETs, bipolar transistors, or the like are provided in the form of IC. An insulating layer is provided between such a substrate and the thin film field effect transistors although such an insulating layer may be dispensed with in the case of the intrinsic silicon substrate.

A gate electrode may be either a single layer electrode or a multi-layer electrode in a gate insulated field effect transistor in accordance with the present invention. The single layer gate electrode may be a silicon electrode doped with phosphorus or an aluminum electrode. The multi-layer gate electrode may be a two-layer electrode which consists of a lower chromium layer and an upper aluminum layer formed thereon or a two-layer electrode which consists of a lower silicon layer doped with phosphorus and an upper metallic or metal silicide layer formed thereon. The aluminum single layer electrode and the upper aluminum layer can be formed by sputtering an aluminum target. The silicon single layer electrode and the lower silicon layer can be formed by low pressure CVD or by sputtering a silicon target doped with phosphorus. The lower chromium layer can be formed by sputtering a chromium target. The metallic layer may be a molybdenum layer

formed by sputtering a molybdenum target, a wolfram layer formed by sputtering a wolfram target, a titanium layer formed by sputtering a titanium target, or an aluminum layer formed by sputtering an aluminum target. The metal silicide layer may be a $MoSi_2$ layer formed by sputtering a $MoSi_2$ target, a WSi_2 layer formed by sputtering a WSi_2 target, or a $TiSi_2$ layer formed by sputtering a $TiSi_2$ target. Although the production method claims as provided infra include several steps, the order of these steps can be changed in accordance with the practical cases and should not limit the scope of patent.

WHAT IS CLAIMED IS:

1. An electro-optical device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising source, drain and channel regions;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor;

an organic resin film provided over said thin film transistor and said interlayer insulating film; and

a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film,

wherein said interlayer insulating film is located between said organic resin film and said channel region of the thin film transistor, and

wherein said thin film transistor comprises silicon and exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon.

2. A device according to claim 1 wherein said pixel electrode is a transparent conductive film.

3. A device according to claim 1 wherein said inorganic material comprises silicon oxide.

4. A device according to claim 1 wherein said channel region comprises a material selected form the group consisting of silicon, germanium and a combination thereof.

5. A device according to claim 1 wherein said interlayer insulating film is 0.2 to 0.6 μm thick.

6. A device according to claim 1 consisting of 640 x 480 pixels arranged in a matrix form.

7. A device according to claim 1 consisting of 1260 x 960 pixels arranged in a matrix form.

8. A device according to claim 1 further comprising a conductive film formed on said interlayer insulating film and electrically connected to said thin film transistor through a contact hole formed in said interlayer insulating film.

9. A device according to claim 8 wherein said pixel electrode is connected to said thin film transistor via said conductive film.

10. An electro-optical device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising source, drain and channel regions;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor;

an organic resin film provided over said thin film transistor and said interlayer insulating film; and

a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film,

wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor,

wherein said thin film transistor comprises silicon and exhibits a peak of Raman spectra, displaced from 522 cm^{-1}.

11. A device according to claim 10 wherein said pixel electrode is a transparent conductive film.

12. A device according to claim 10 wherein said inorganic material comprises silicon oxide.

13. A device according to claim 10 wherein said channel region comprises a material selected from the group consisting of silicon, germanium and a combination thereof.

14. A device according to claim 10 wherein said interlayer insulating film is 0.2 to 0.6 μm thick.

15. A device according to claim 10 consisting of 640 x 480 pixels arranged in a matrix form.

16. A device according to claim 10 consisting of 1260 x 960 pixels arranged in a matrix form.

17. A device according to claim 10 further comprising a conductive film formed on said interlayer insulating film and electrically connected to said thin film transistor through a contact hole formed in said interlayer insulating film.

18. A device according to claim 17 wherein said pixel electrode is connected to said thin film transistor via said conductive film.

19. An electro-optical device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a crystalline semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region; and

a gate electrode adjacent to said channel region;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said thin film transistor and said interlayer insulating film;

wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor,

wherein said thin film transistor comprises silicon and exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon.

20. A device according to claim 19 further comprising a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film.

21. A device according to claim 20 wherein said pixel electrode is a transparent conductive film.

22. A device according to claim 19 wherein said inorganic material comprises silicon oxide.

23. A device according to claim 19 wherein said channel region comprises a material selected from the group consisting of silicon, germanium and a combination thereof.

24. A device according to claim 19 wherein said gate insulating film is 500Å to 2000Å thick.

25. A device according to claim 19 wherein said interlayer insulating film is 0.2 to 0.6 μm thick.

26. A device according to claim 19 consisting of 640 x 480 pixels arranged in a matrix form.

27. A device according to claim 19 consisting of 1260 x 960 pixels arranged in a matrix form.

28. A device according to claim 19 wherein said crystalline semiconductor layer has an electron mobility not lower than 15 $cm^2/Vsec$.

29. A device according to claim 19 wherein said crystalline semiconductor layer has a hole mobility not lower than 10 $cm^2/Vsec$.

30. A device according to claim 19 further comprising a conductive film formed on said interlayer insulating film and electrically connected to said thin film transistor through a contact hole formed in said interlayer insulating film.

31. A device according to claim 30 wherein said pixel electrode is connected to said thin film transistor via said conductive film.

32. An electro-optical device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a crystalline semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said thin film transistor and said interlayer insulating film;

wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor, and

wherein said semiconductor layer comprises silicon and exhibits a peak of Raman spectra, displaced from 522 cm^{-1}.

33. A device according to claim 32 further comprising a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film.

34. A device according to claim 33 wherein said pixel electrode is a transparent conductive film.

35. A device according to claim 32 wherein said inorganic material comprises silicon oxide.

36. A device according to claim 32 wherein said channel region comprises a material selected from the group consisting of silicon, germanium and a combination thereof.

37. A device according to claim 32 wherein said gate insulating film is 500Å to 2000Å thick.

38. A device according to claim 32 wherein said interlayer insulating film is 0.2 to 0.6 μm thick.

39. A device according to claim 32 consisting of 640 x 480 pixels arranged in a matrix form.

40. A device according to claim 32 consisting of 1260 x 960 pixels arranged in a matrix form.

41. A device according to claim 32 wherein said crystalline semiconductor layer has an electron mobility not lower than 15 $cm^2/Vsec$.

42. A device according to claim 32 wherein said crystalline semiconductor layer has a hole mobility not lower than 10 $cm^2/Vsec$.

43. A device according to claim 32 further comprising a conductive film formed on said interlayer insulating film and electrically connected to said thin film transistor through a contact hole formed in said interlayer insulating film.

44. A device according to claim 43 wherein said pixel electrode is connected to said thin film transistor via said conductive film.

45. An electro-optical device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least an n-channel thin film transistor and at least a p-channel thin film transistor both formed over said first substrate, each of said n-channel and p-channel thin film transistors comprising:

a crystalline semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region; and

a gate electrode adjacent to said channel region;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said thin film transistor and said interlayer insulating film;

wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor,

wherein said thin film transistor comprises silicon and exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon.

46. A device according to claim 45 further comprising a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film.

47. A device according to claim 46 wherein said pixel electrode is a transparent conductive film.

48. A device according to claim 45 wherein said inorganic material comprises silicon oxide.

49. A device according to claim 45 wherein said channel region comprises a material selected from the group consisting of silicon, germanium and a combination thereof.

50. A device according to claim 45 wherein said gate insulating film is 500Å to 2000Å thick.

51. A device according to claim 45 wherein said interlayer insulating film is 0.2 to 0.6 μm thick.

52. A device according to claim 45 consisting of 640 x 480 pixels arranged in a matrix form.

53. A device according to claim 45 consisting of 1260 x 960 pixels arranged in a matrix form.

54. A device according to claim 45 wherein said crystalline semiconductor layer has an electron mobility not lower than 15 $cm^2/Vsec$.

55. A device according to claim 45 wherein said crystalline semiconductor layer has a hole mobility not lower than 10 $cm^2/Vsec$.

56. A device according to claim 45 further comprising a conductive film formed on said interlayer insulating film and electrically connected to said thin film transistor through a contact hole formed in said interlayer insulating film.

57. A device according to claim 56 wherein said pixel electrode is connected to said thin film transistor via said conductive film.

58. A device according to claim 1, wherein said organic resin film comprises polyimide.

59. A device according to claim 10, wherein said organic resin film comprises polyimide.

60. A device according to claim 19, wherein said organic resin film comprises polyimide.

61. A device according to claim 32, wherein said organic resin film comprises polyimide.

62. A device according to claim 45, wherein said organic resin film comprises polyimide.

63. A device according to claim 1, wherein said channel region comprises boron at concentration in a range of 1×10^{15} - 1×10^{18} cm^{-3}.

64. A device according to claim 10, wherein said channel region comprises boron at concentration in a range of 1×10^{15} - 1×10^{18} cm^{-3}.

65. A device according to claim 19, wherein said channel region comprises boron at concentration in a range of 1×10^{15} - 1×10^{18} cm^{-3}.

66. A device according to claim 32, wherein said channel region comprises boron at concentration in a range of 1×10^{15} - 1×10^{18} cm^{-3}.

67. A device according to claim 45, wherein said channel region of each of the n-channel and p-channel thin film transistors comprises boron at concentration in a range of 1×10^{15} - 1×10^{18} cm^{-3}.

ABSTRACT OF THE DISCLOSURE

A grey tone display and a driving method are described. The display comprises a light influencing layer, an electrode pad located adjacent to the layer at one side of the layer in order to define a pixel in the layer, an n-channel field effect transistors connected to the electrode pad at its source terminal, a p-channel field effect transistors connected to the electrode pad at its source terminal, a first control line connected to the drain terminal of the n-channel field effect transistor, a second control line connected to the drain terminal of the p-channel field effect transistor, a third control line connected to the gate terminals of the n-channel field effect transistor and the p-channel field effect transistor, and a control circuit for supplying control signals to the first, second and third control lines. By this configuration, the voltage of the electrode pad can be arbitrarily controlled by adjusting the input level at the gate terminals.

FIG. 1

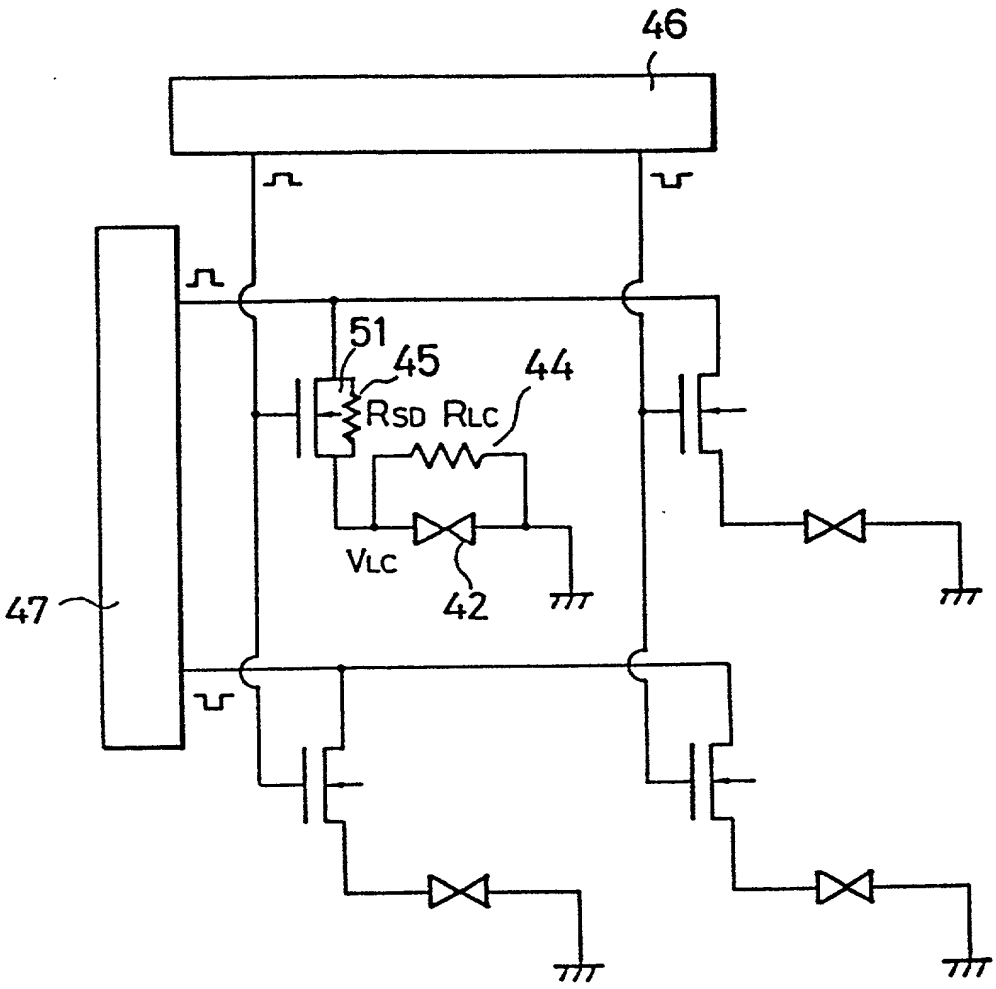


FIG. 2

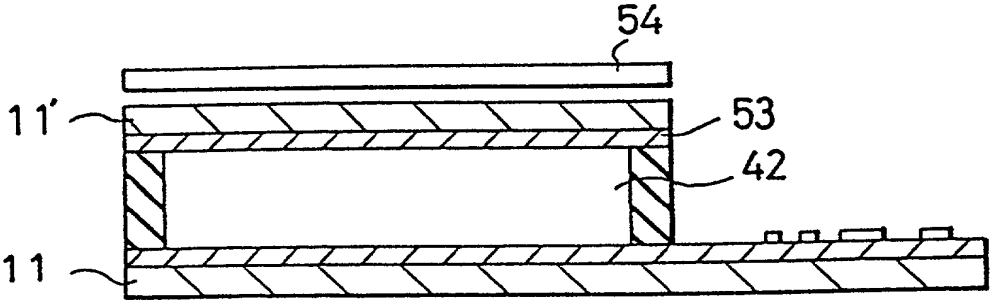


FIG. 3

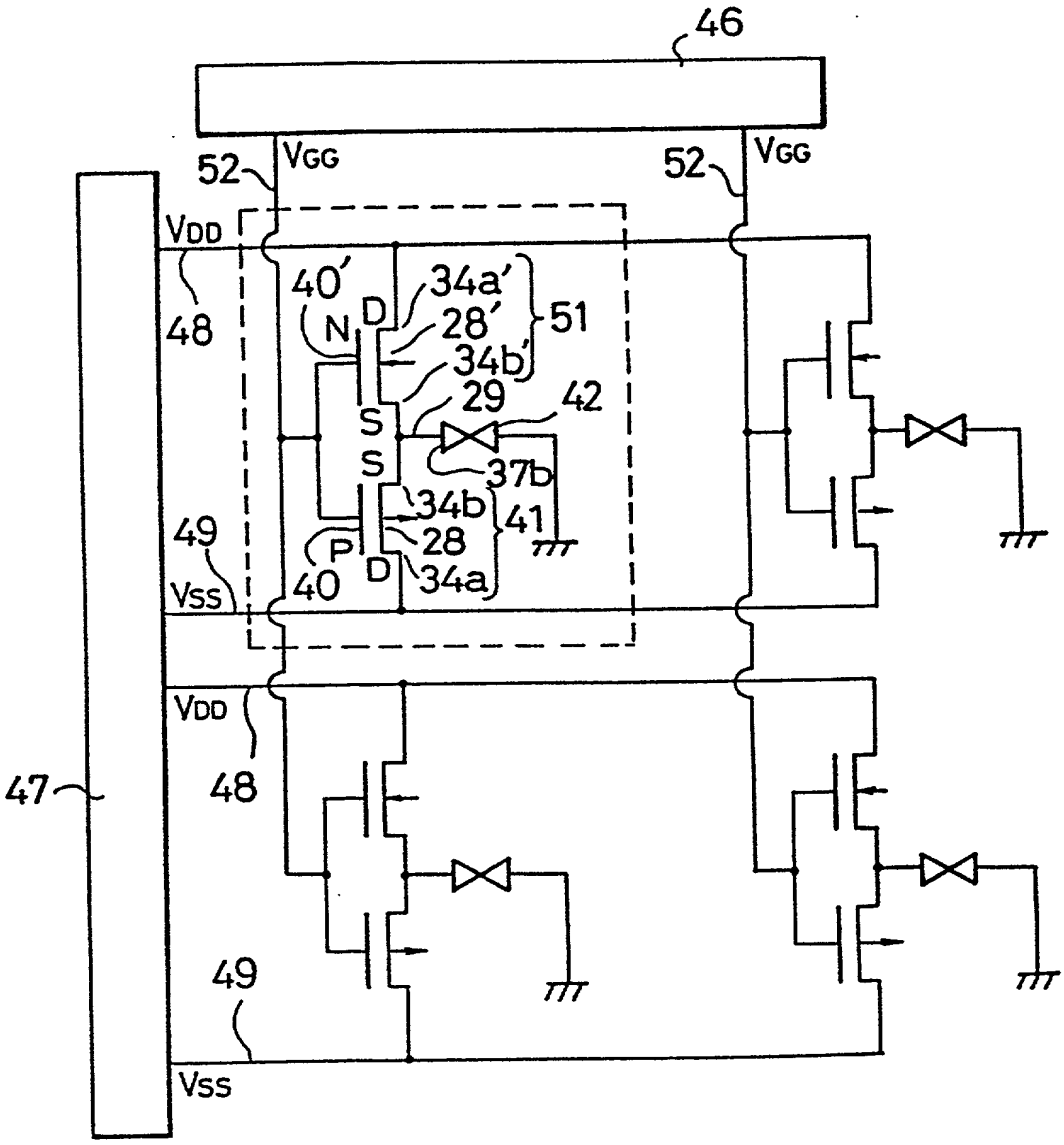

46
52
VGG
52
VGG
VDD
48
40'
N
D
34a'
28'
51
34b'
29
42
S
S
37b
34b
41
49
P
D
28
34a
Vss
40
VDD
48
47
49
Vss

FIG. 4 (A)

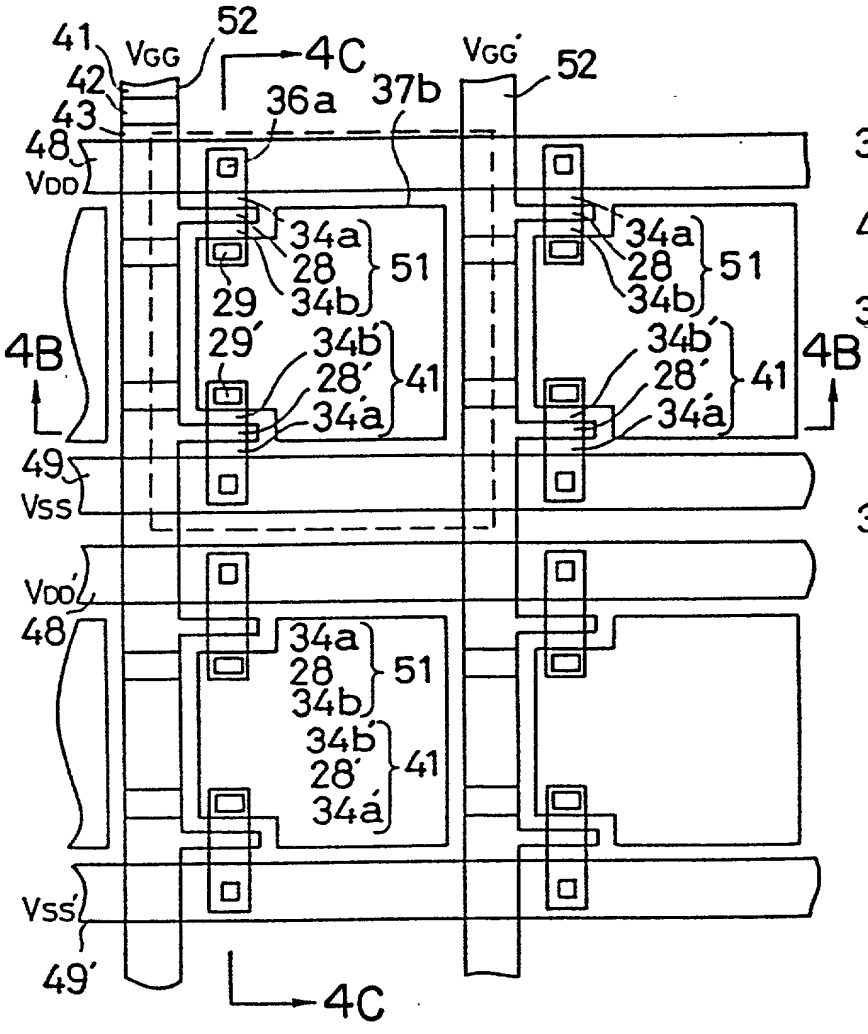


FIG. 4 (C)

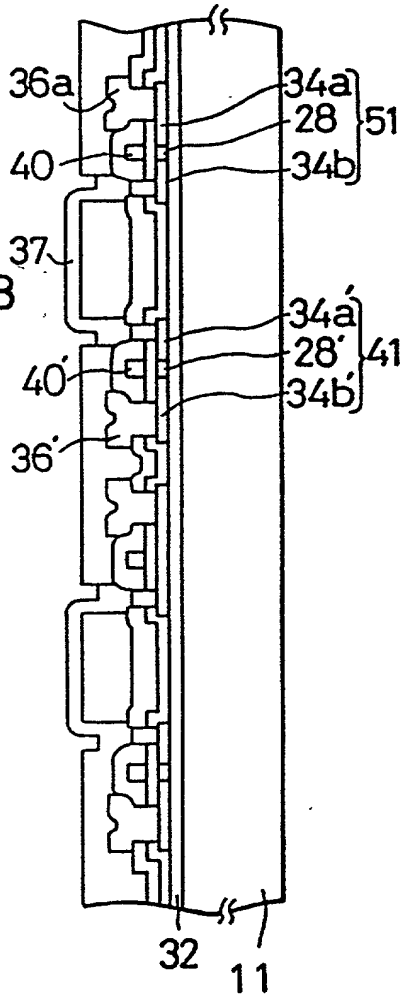


FIG. 4 (B)

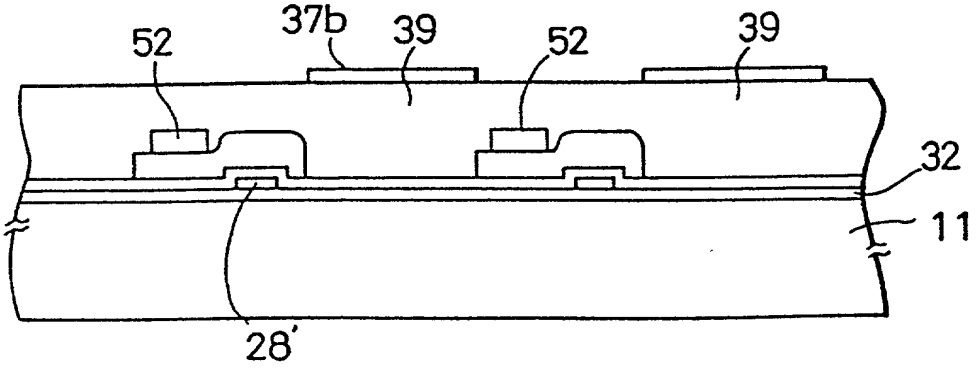


FIG. 5 (A)

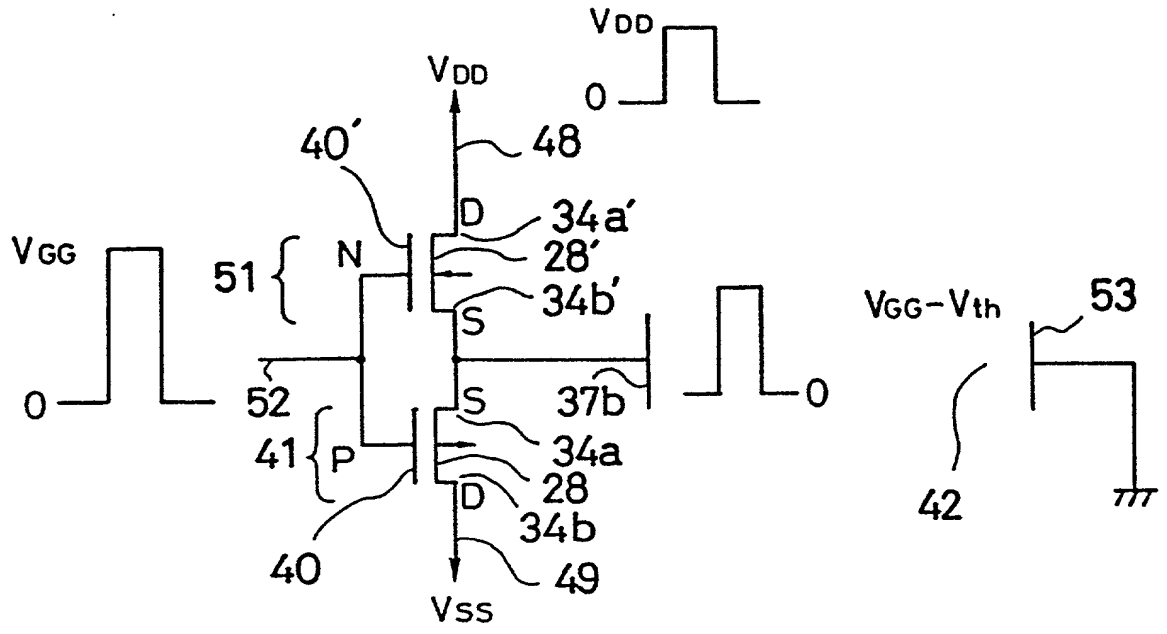

VDD
VDD
0
40'
48
D
34a'
VGG
51
N
28'
34b'
S
0
52
S
37b
0
41
P
34a
28
D
34b
40
49
Vss
VGG-Vth
53
42

FIG. 5 (B)

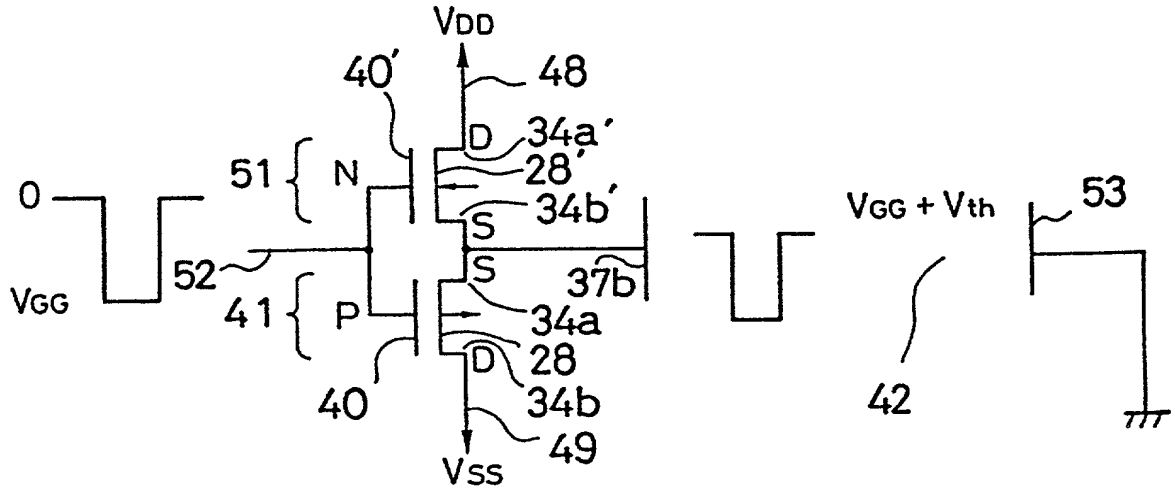

VDD
40'
48
D
34a'
0
51
N
28'
34b'
S
52
S
37b
VGG
41
P
34a
28
D
40
34b
49
Vss
VGG + Vth
53
42

FIG. 6

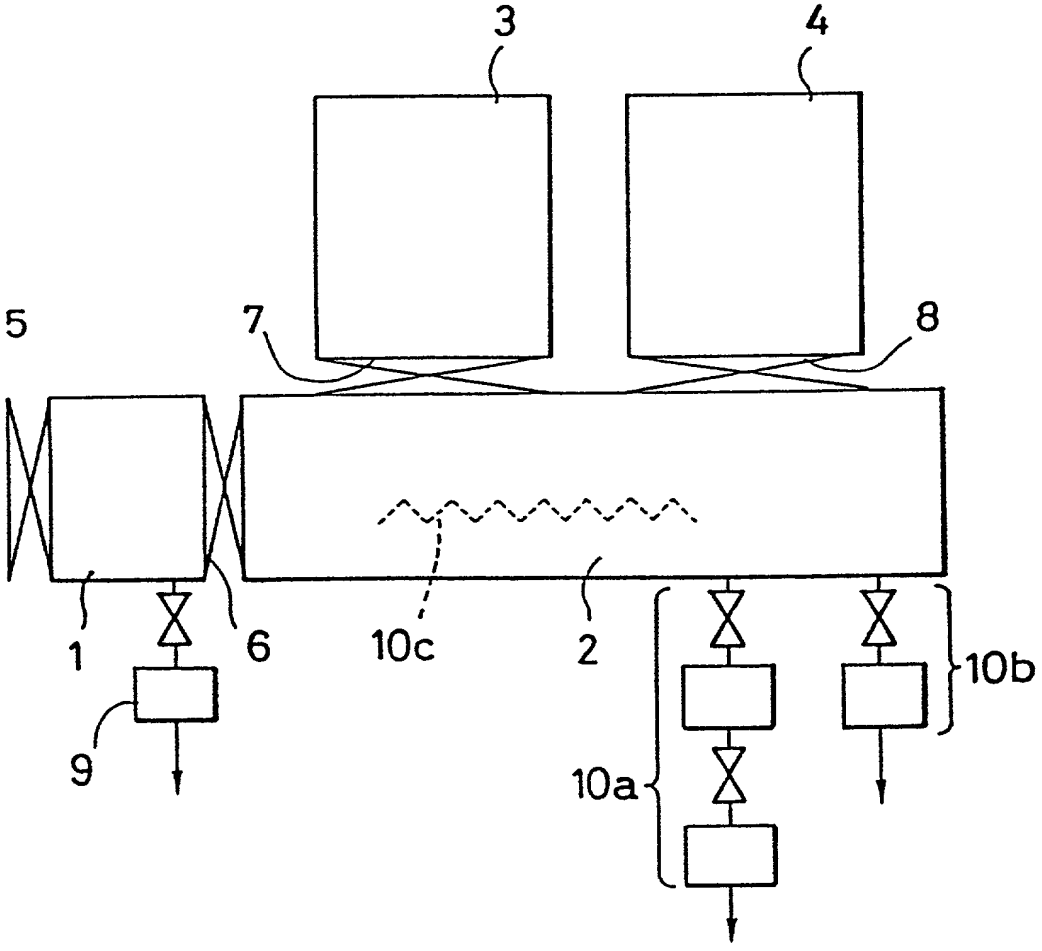


FIG. 7 (A)

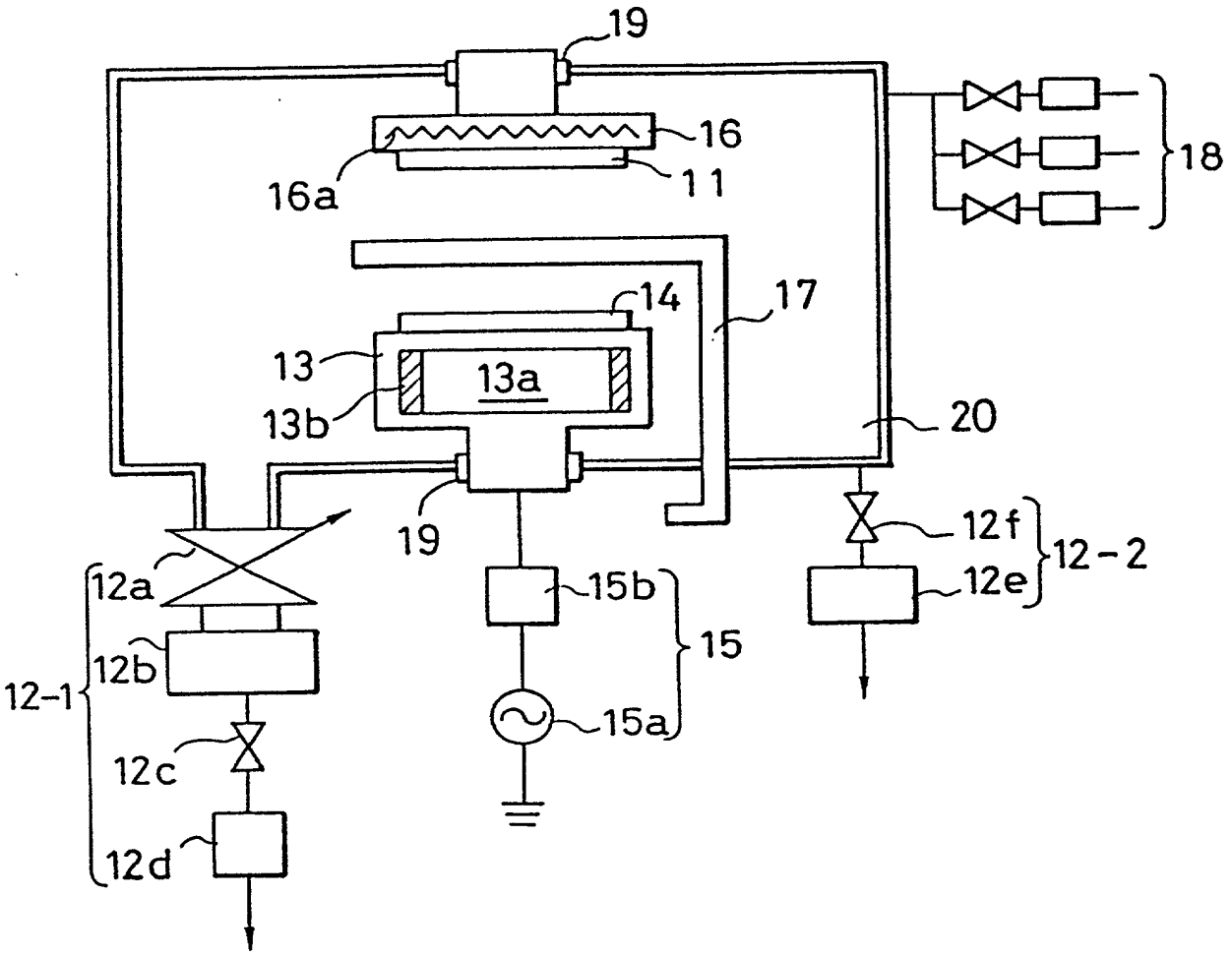

19
16
16a
11
18
14
17
13
13a
13b
20
19
12f
12-2
12e
12a
15b
15
12b
12-1
15a
12c
12d

FIG. 7 (B)

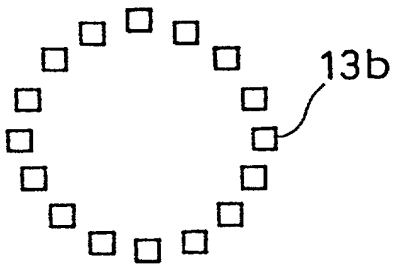

13b

FIG. 8 (A)

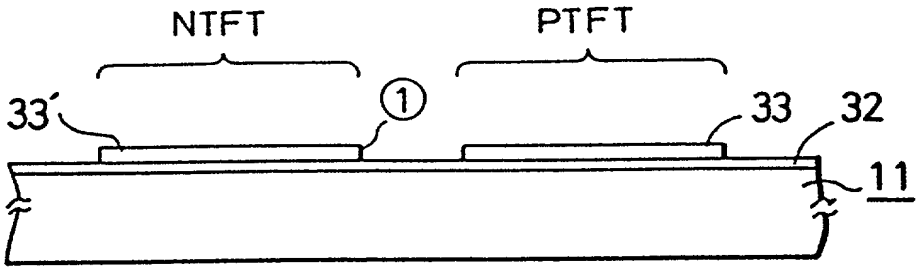


FIG. 8 (B)

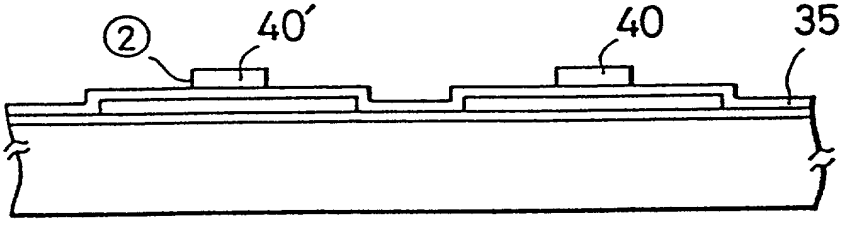


FIG. 8 (C)

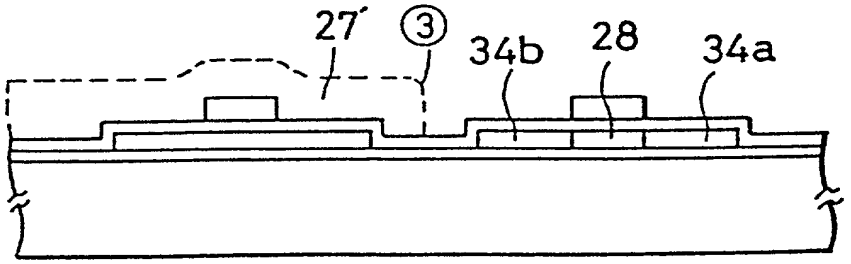


FIG. 8 (D)

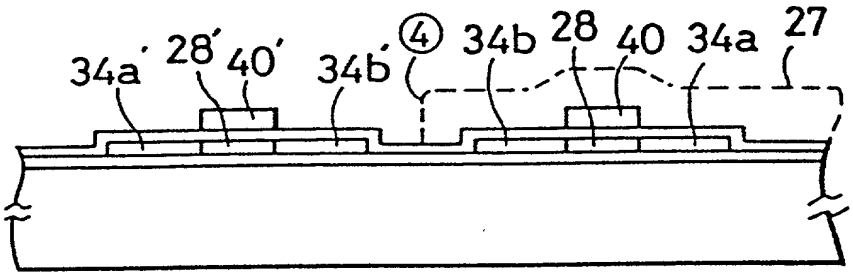


FIG. 8 (E)

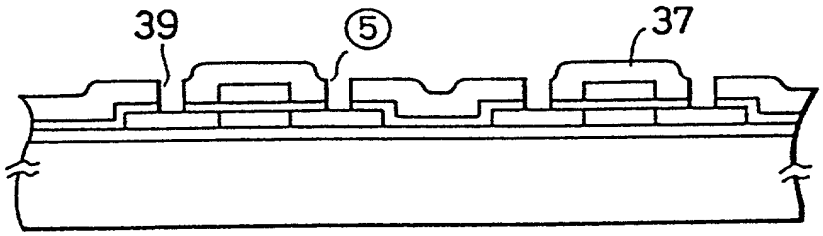


FIG. 8 (F)

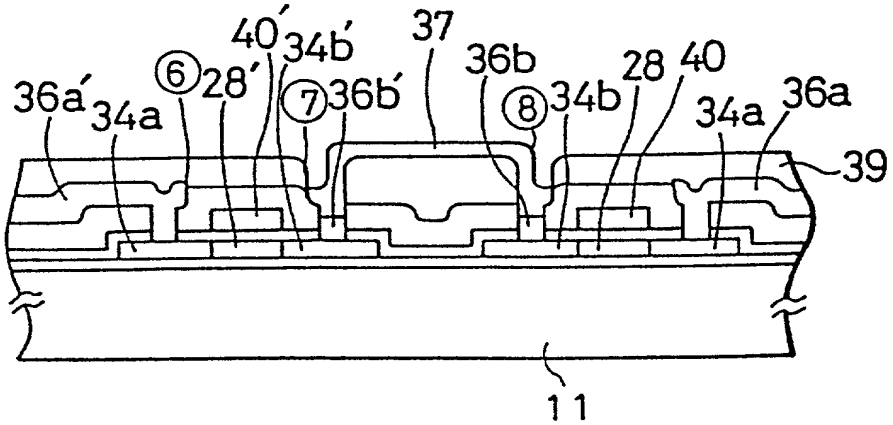


FIG. 9 (A)

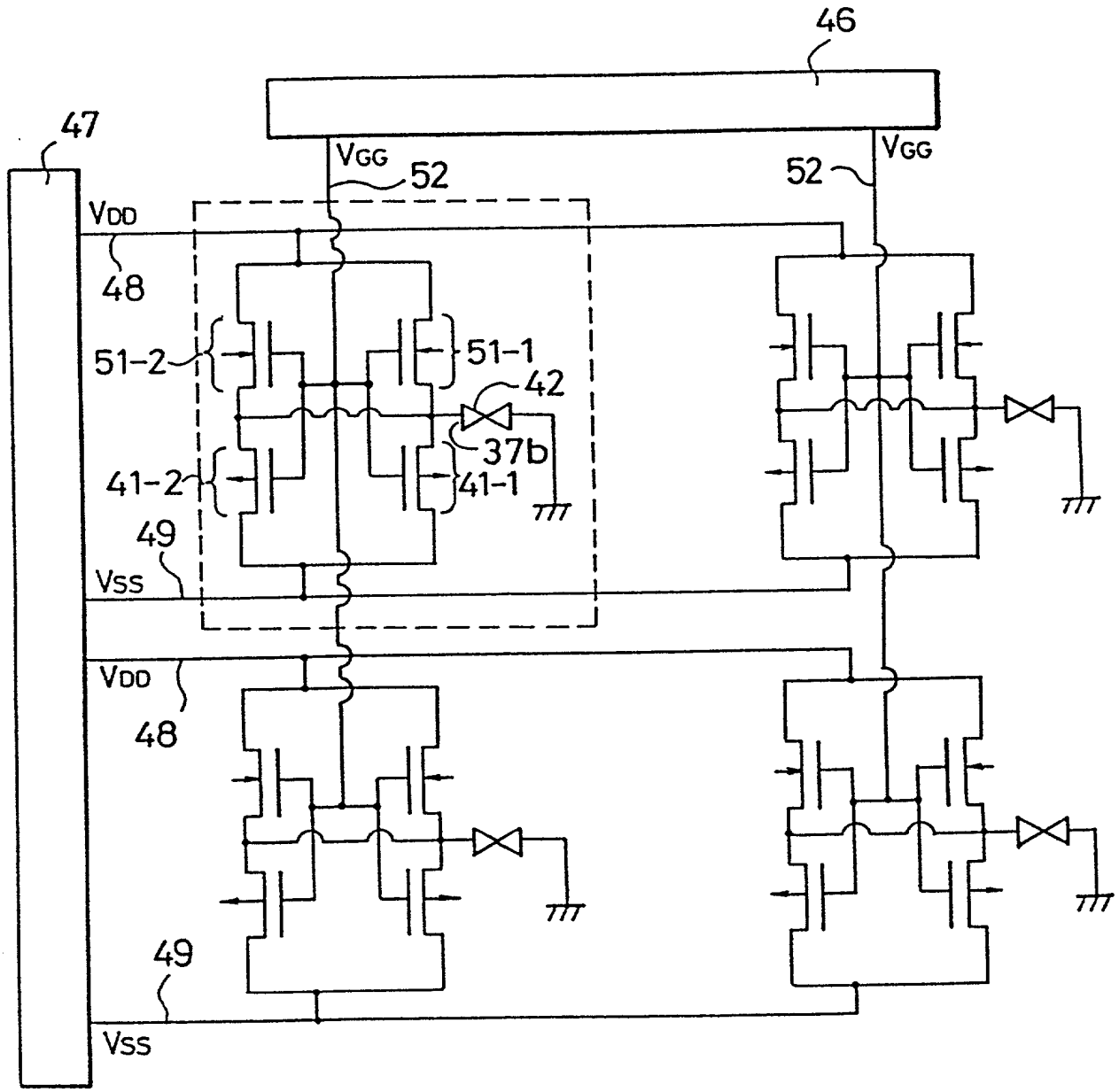

46
47
VGG
52
52
VGG
VDD
48
51-2
51-1
42
37b
41-2
41-1
49
Vss
VDD
48
49
Vss

FIG. 9 (B)

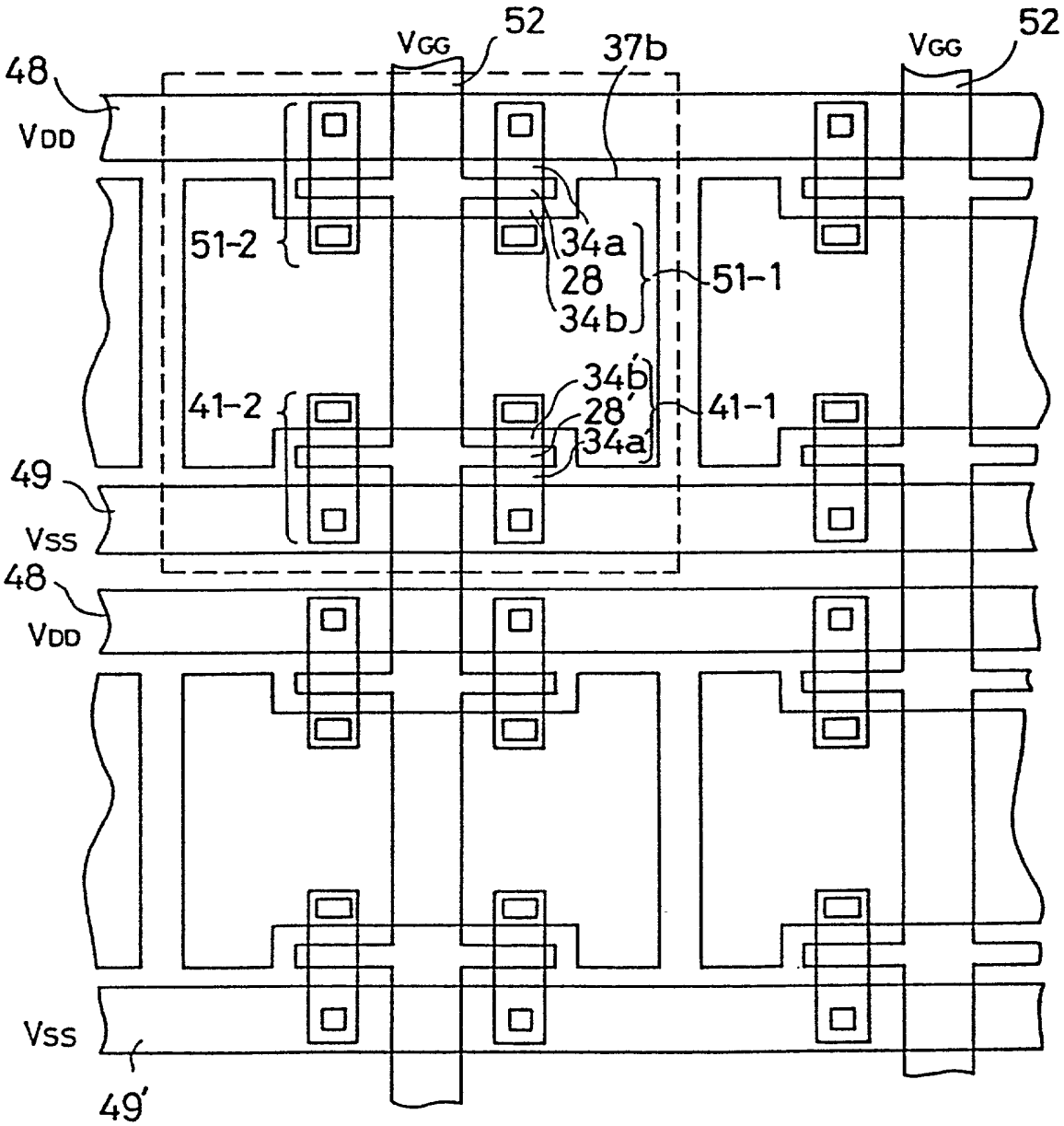

48
VDD
VGG
52
37b
VGG
52
51-2
34a
28
34b
51-1
41-2
34b'
28'
34a'
41-1
49
Vss
48
VDD
Vss
49'

FIG. 10 (A)

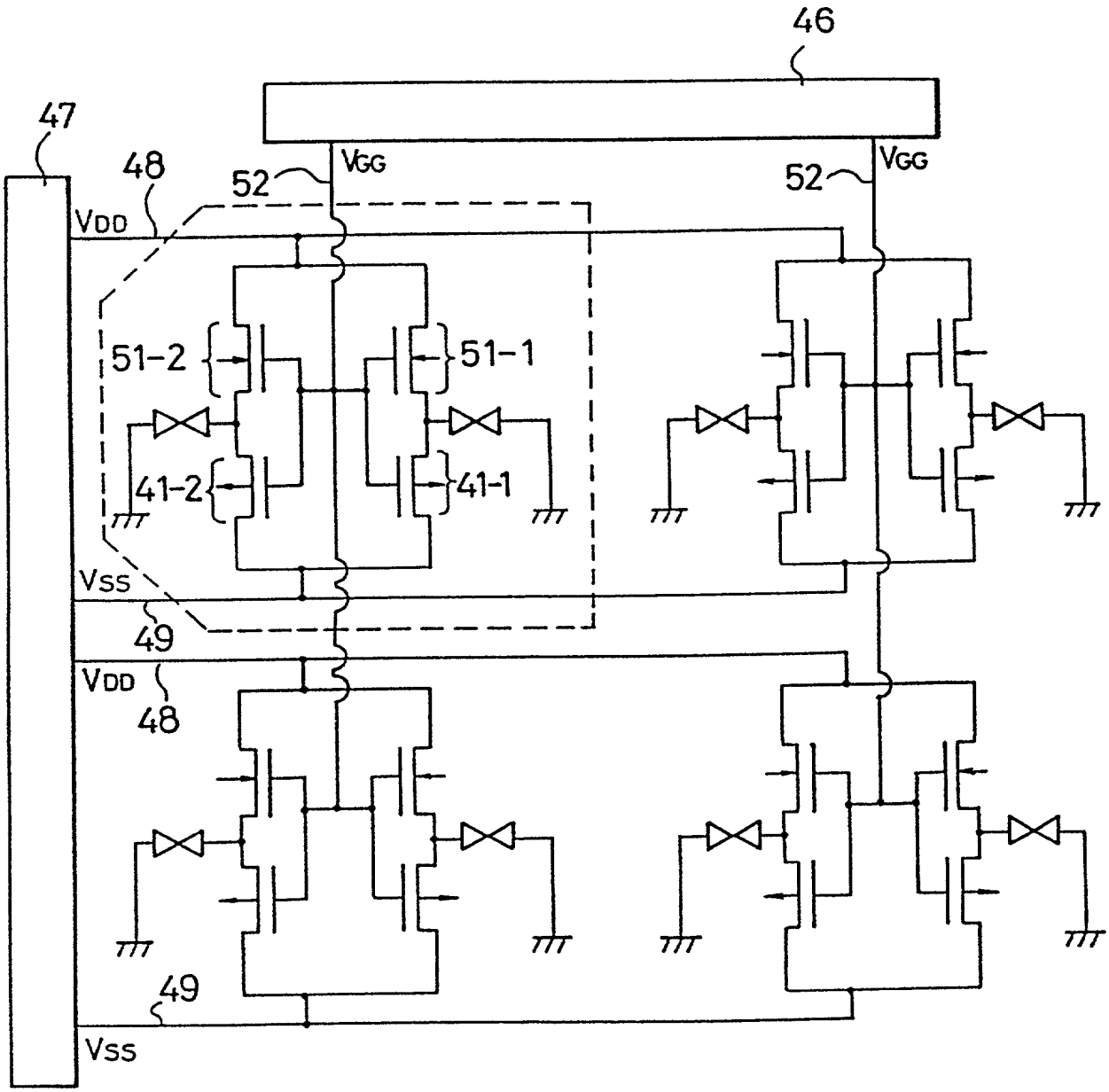


FIG. 10 (B)

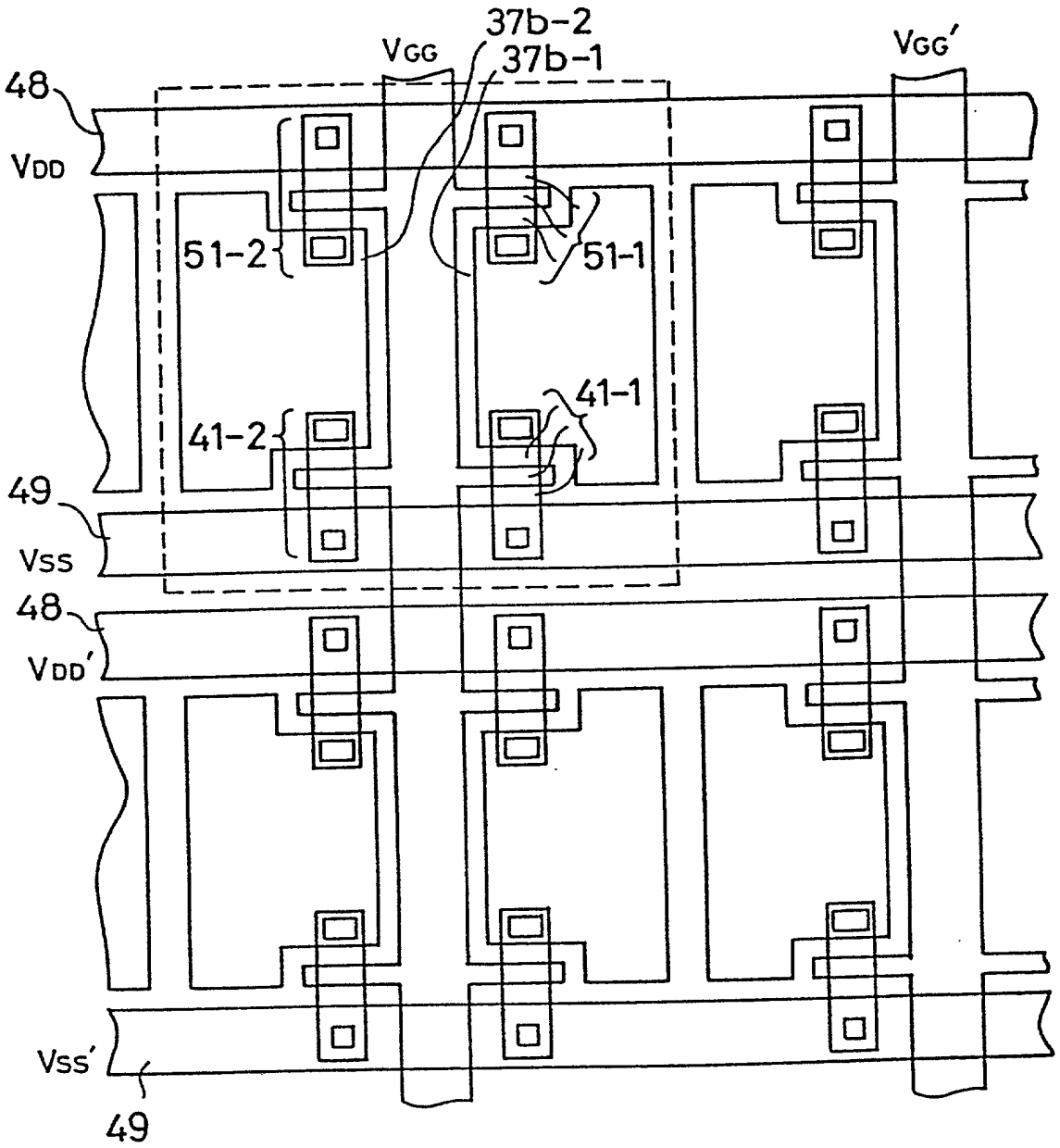


FIG. 11

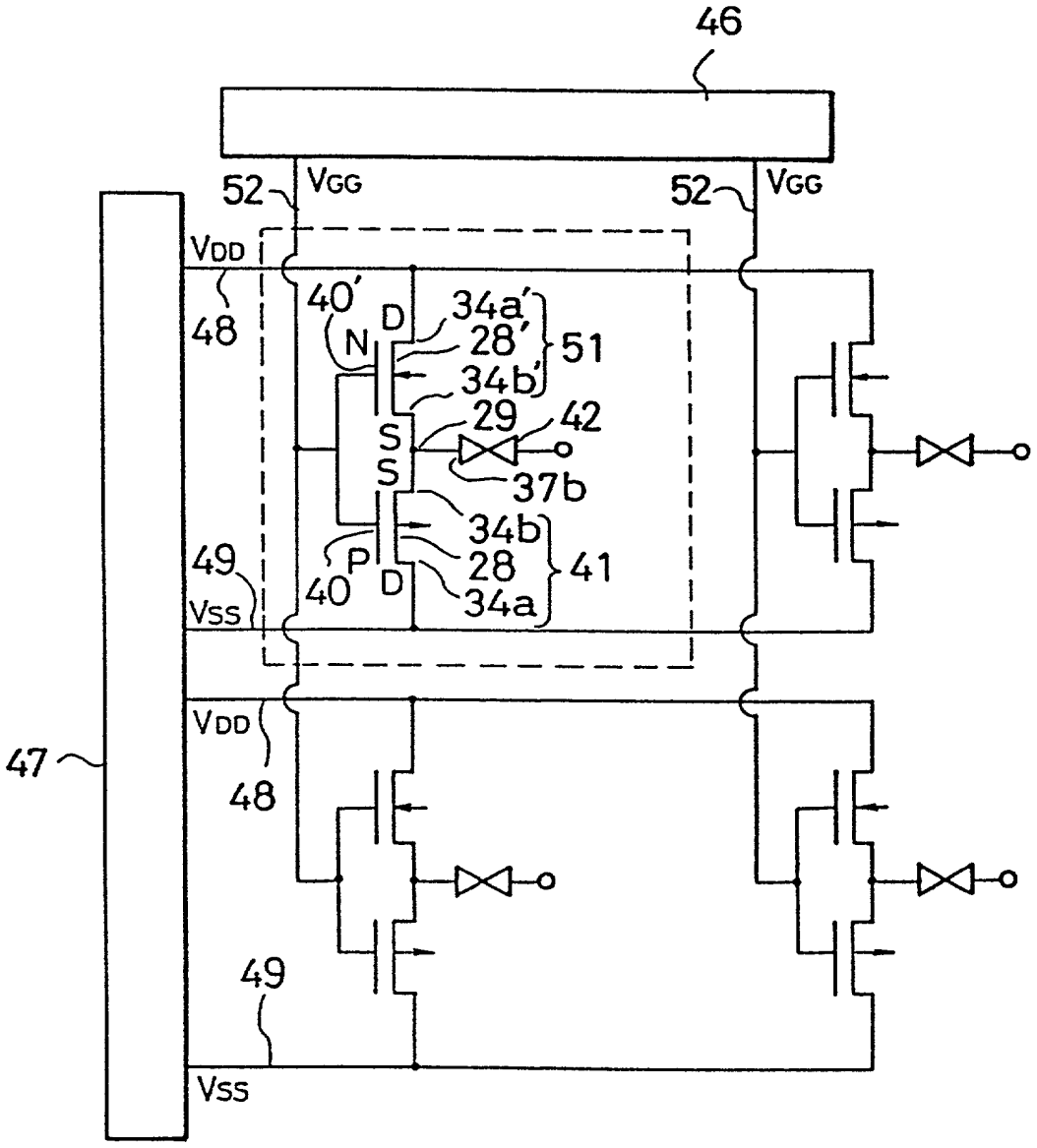

46
52
VGG
52
VGG
VDD
48
40'
N
D
34a'
28'
51
34b'
29
42
S
S
37b
34b
28
34a
41
49
VSS
40
P
D
VDD
48
47
49
VSS

FIG. 12

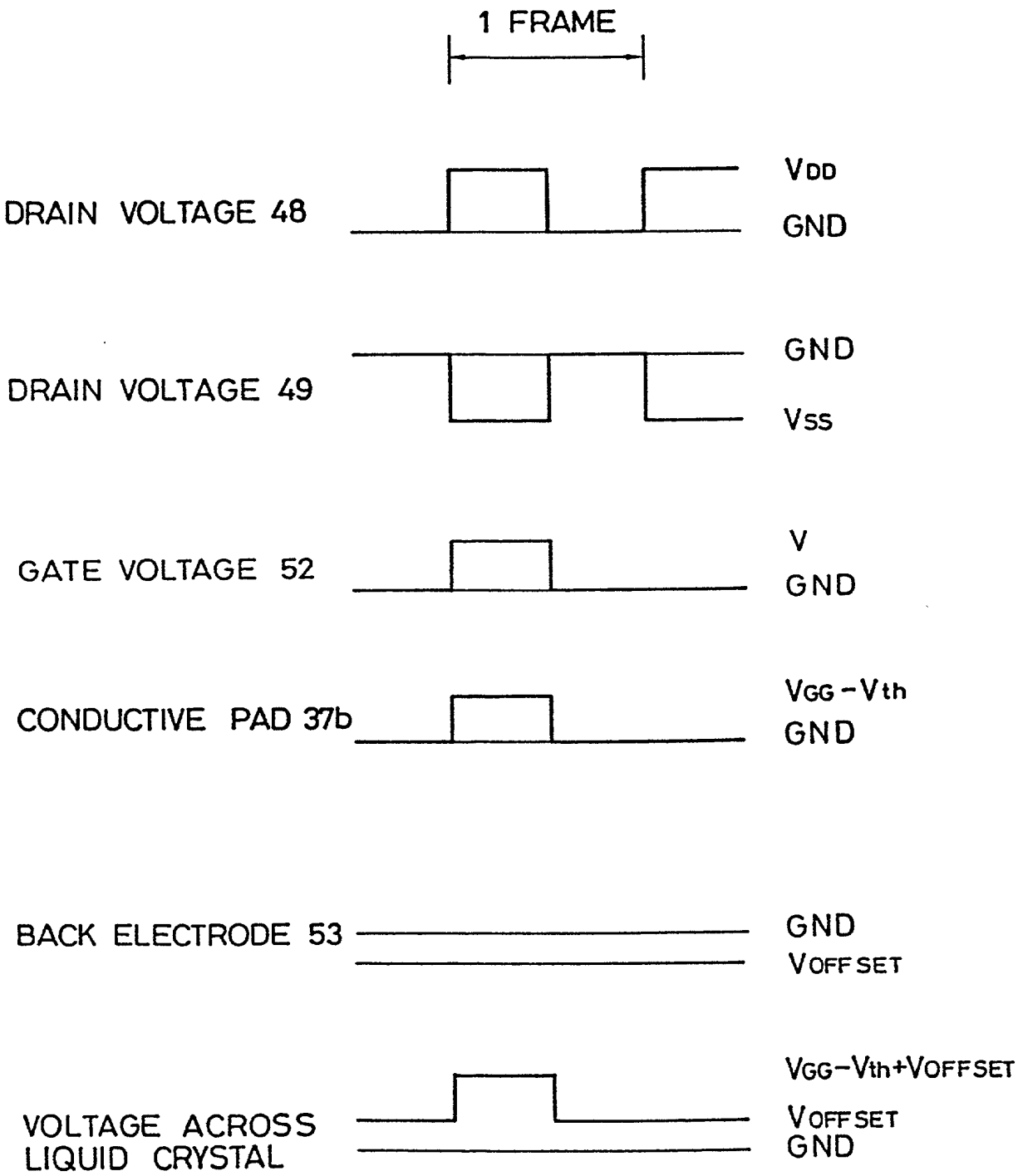

1 FRAME
DRAIN VOLTAGE 48
VDD
GND
DRAIN VOLTAGE 49
GND
VSS
GATE VOLTAGE 52
V
GND
CONDUCTIVE PAD 37b
VGG-Vth
GND
BACK ELECTRODE 53
GND
VOFFSET
VOLTAGE ACROSS LIQUID CRYSTAL
VGG-Vth+VOFFSET
VOFFSET
GND

FIG. 13

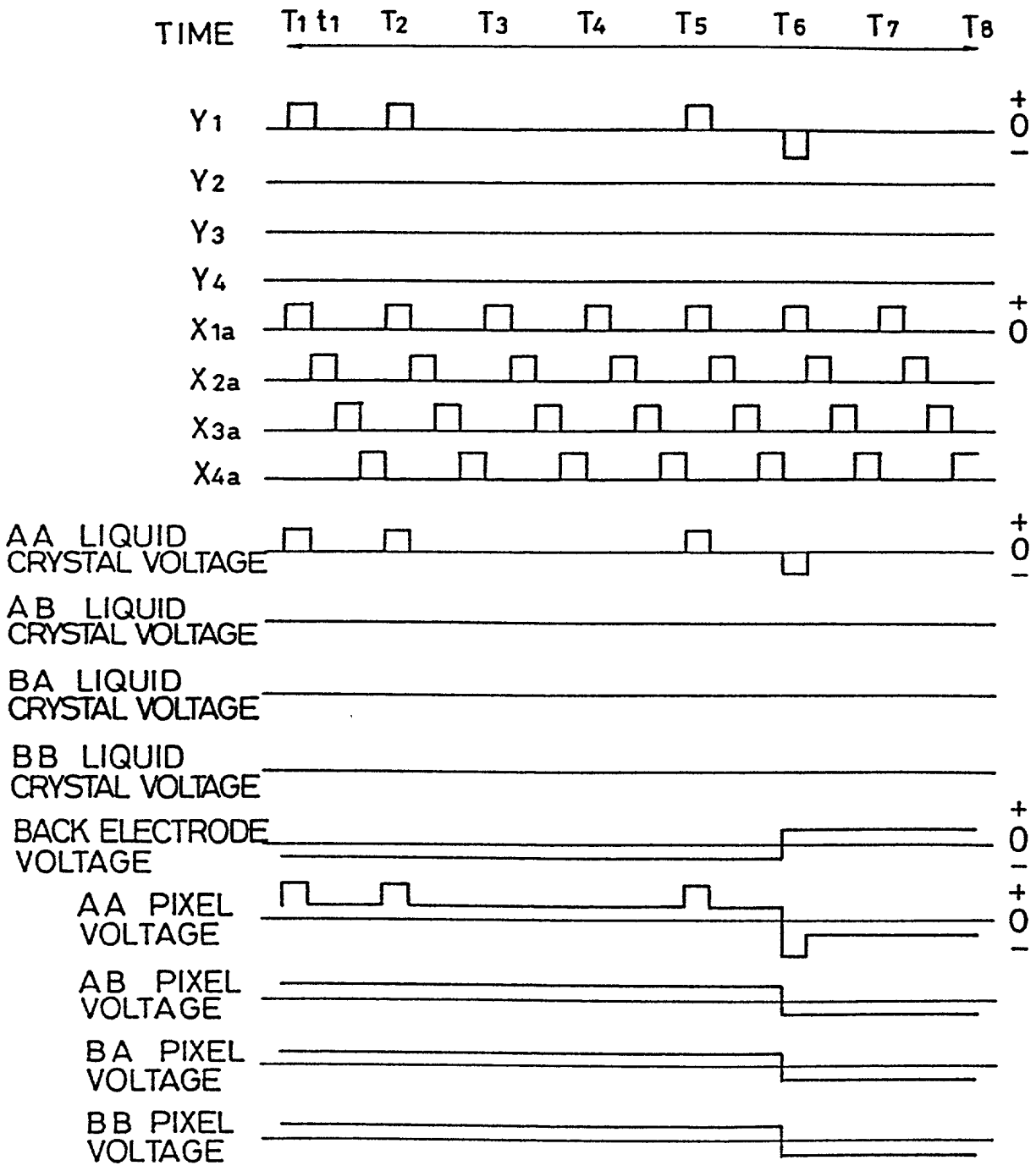

TIME
T1 t1
T2
T3
T4
T5
T6
T7
T8
Y1
Y2
Y3
Y4
X1a
X2a
X3a
X4a
+
0
−
AA LIQUID CRYSTAL VOLTAGE
AB LIQUID CRYSTAL VOLTAGE
BA LIQUID CRYSTAL VOLTAGE
BB LIQUID CRYSTAL VOLTAGE
BACK ELECTRODE VOLTAGE
AA PIXEL VOLTAGE
AB PIXEL VOLTAGE
BA PIXEL VOLTAGE
BB PIXEL VOLTAGE

FIG. 14

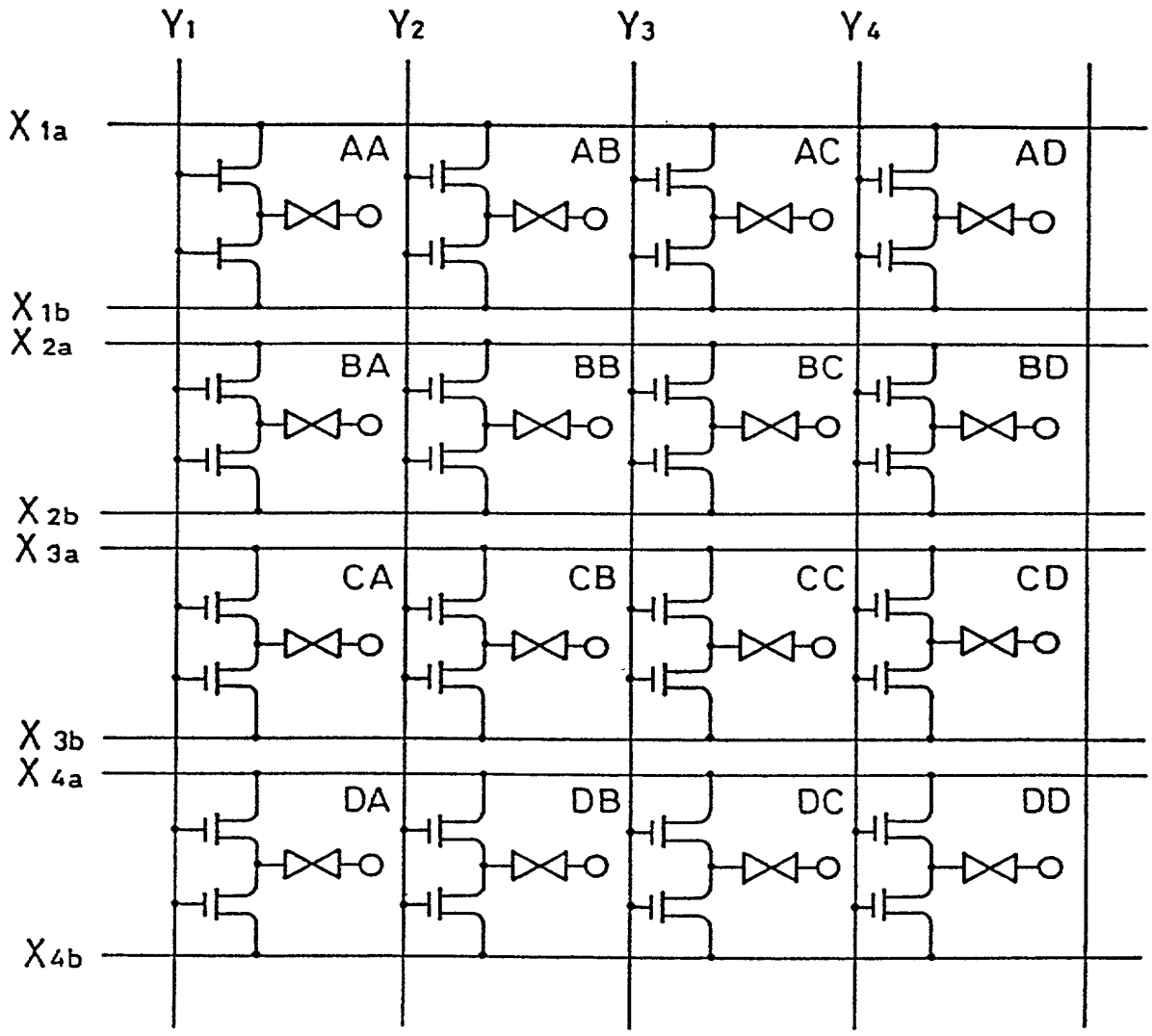

Y1
Y2
Y3
Y4
X 1a
X 1b
X 2a
X 2b
X 3a
X 3b
X 4a
X4b
AA
AB
AC
AD
BA
BB
BC
BD
CA
CB
CC
CD
DA
DB
DC
DD

FIG. 15

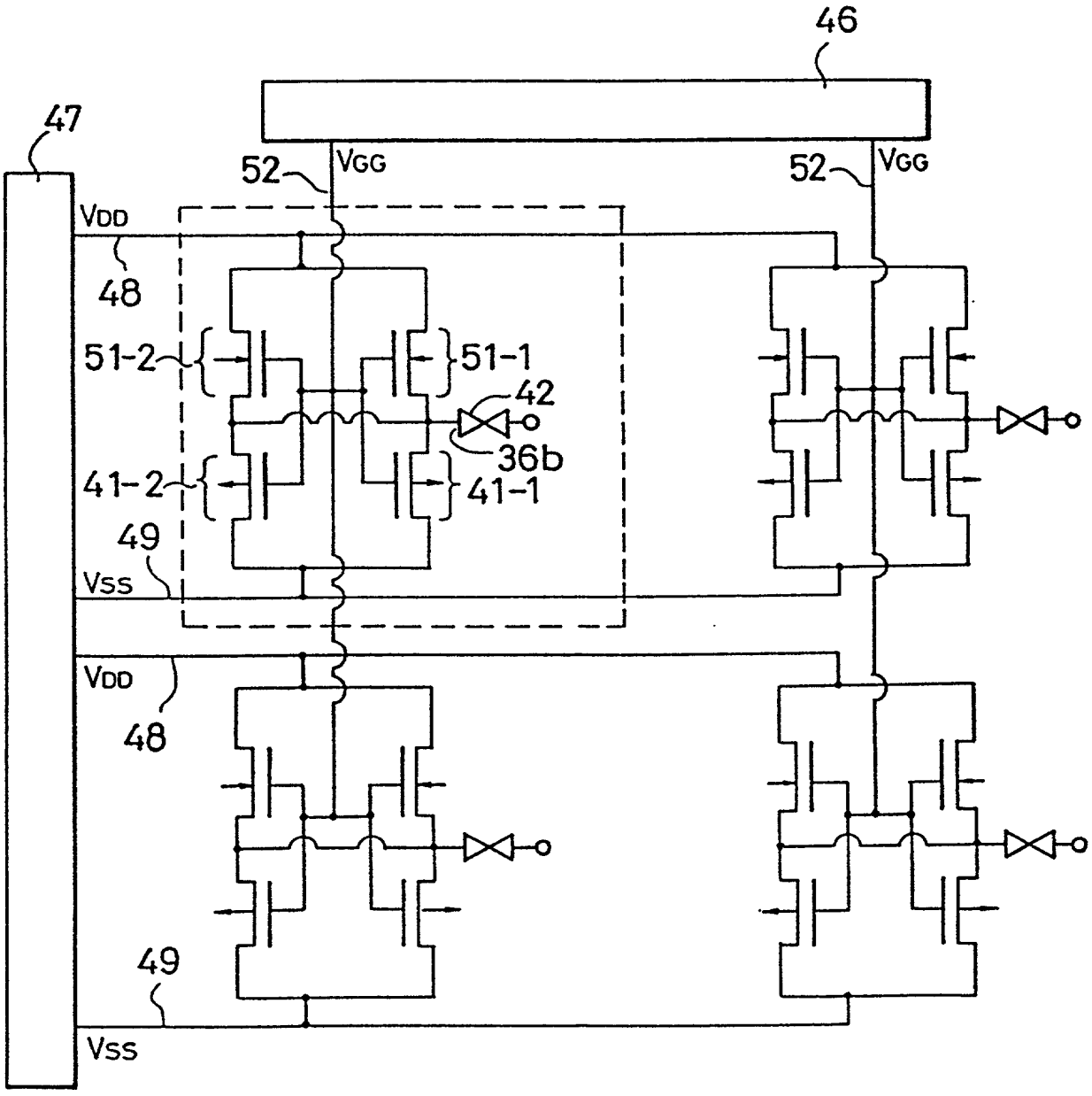

46
47
52
VGG
52
VGG
VDD
48
51-2
51-1
42
36b
41-2
41-1
49
Vss
VDD
48
49
Vss

FIG. 16

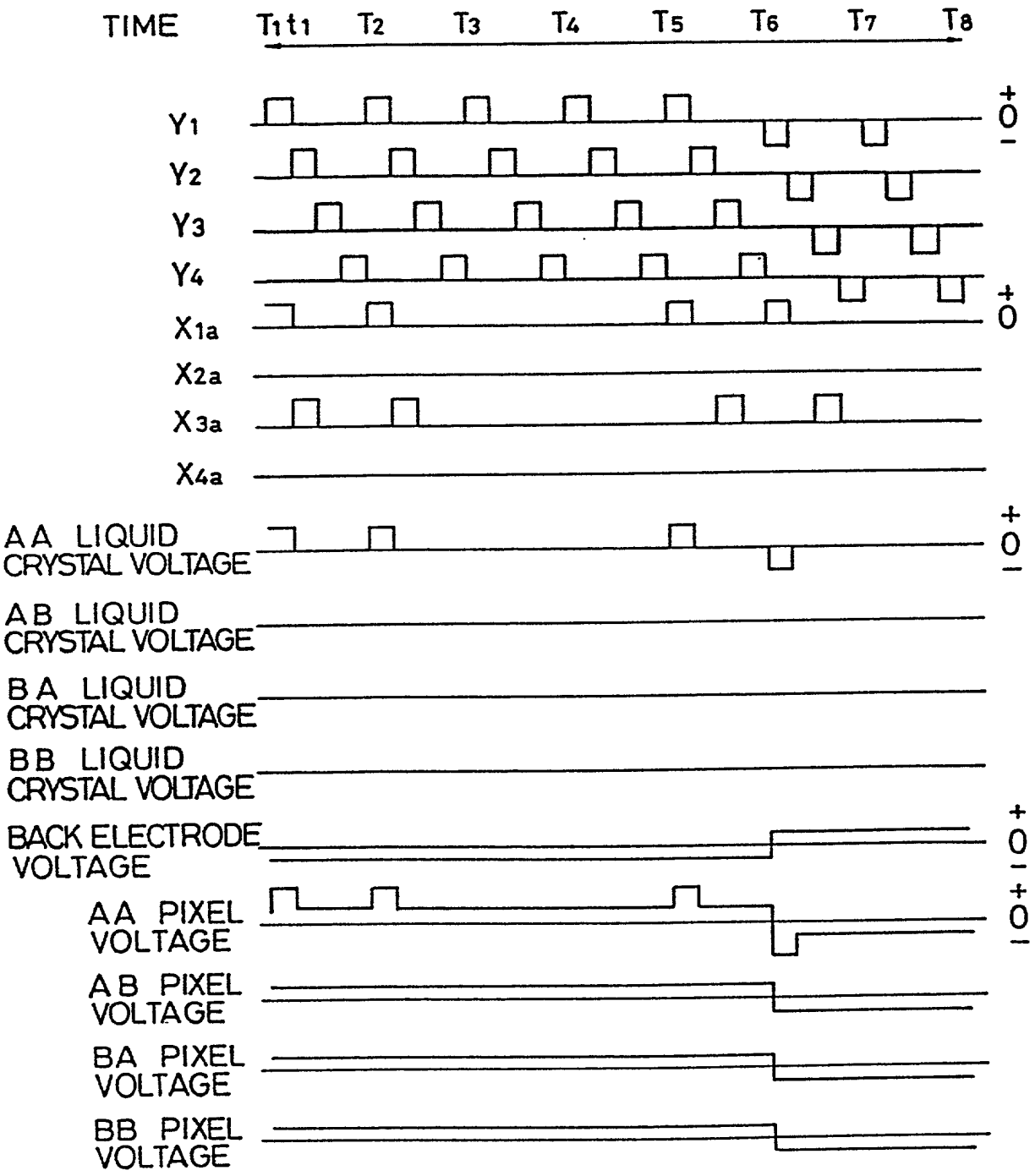

TIME
T1 t1
T2
T3
T4
T5
T6
T7
T8
Y1
Y2
Y3
Y4
X1a
X2a
X3a
X4a
+
0
−
AA LIQUID CRYSTAL VOLTAGE
AB LIQUID CRYSTAL VOLTAGE
BA LIQUID CRYSTAL VOLTAGE
BB LIQUID CRYSTAL VOLTAGE
BACK ELECTRODE VOLTAGE
AA PIXEL VOLTAGE
AB PIXEL VOLTAGE
BA PIXEL VOLTAGE
BB PIXEL VOLTAGE

FIG. 17

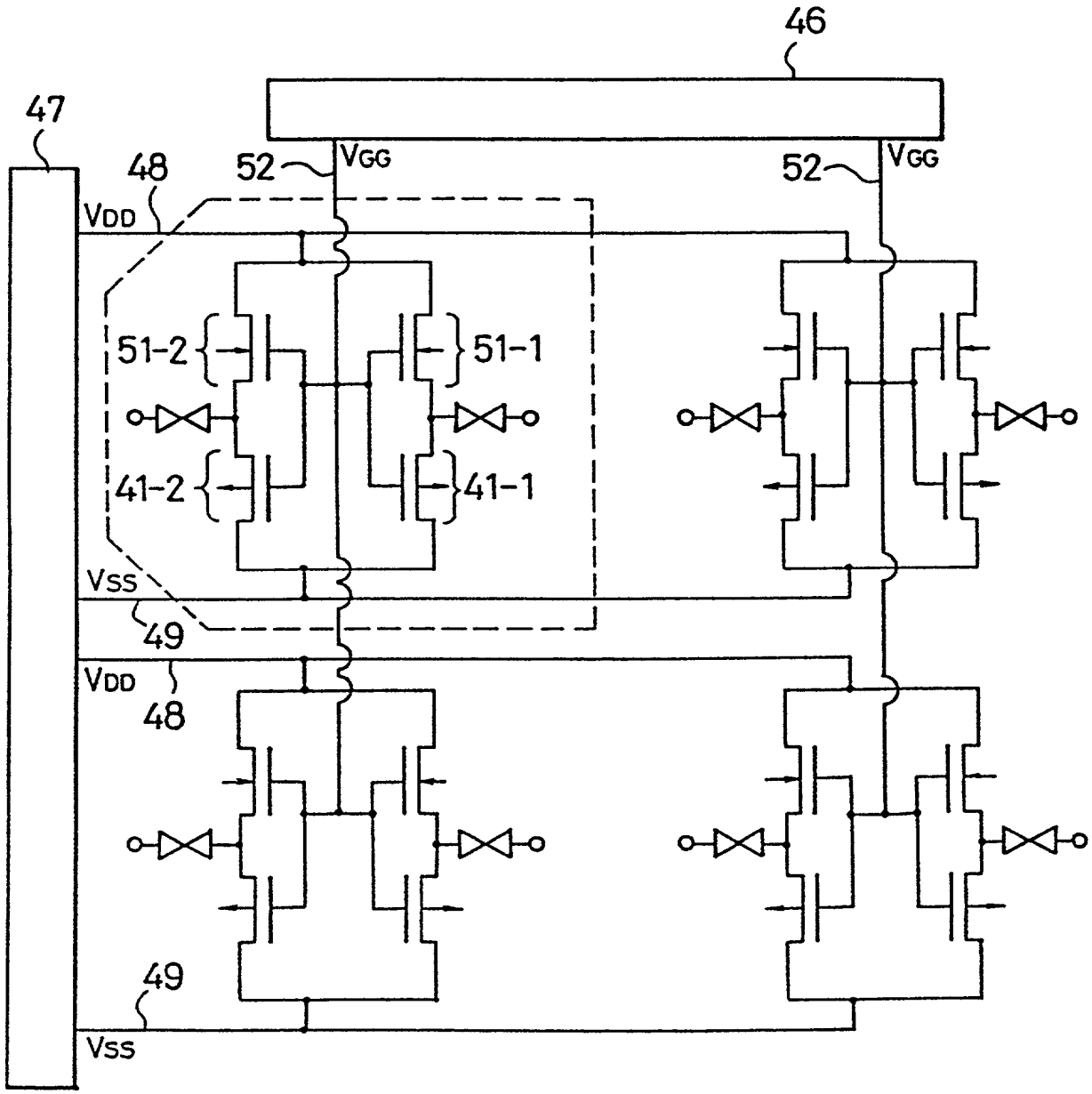
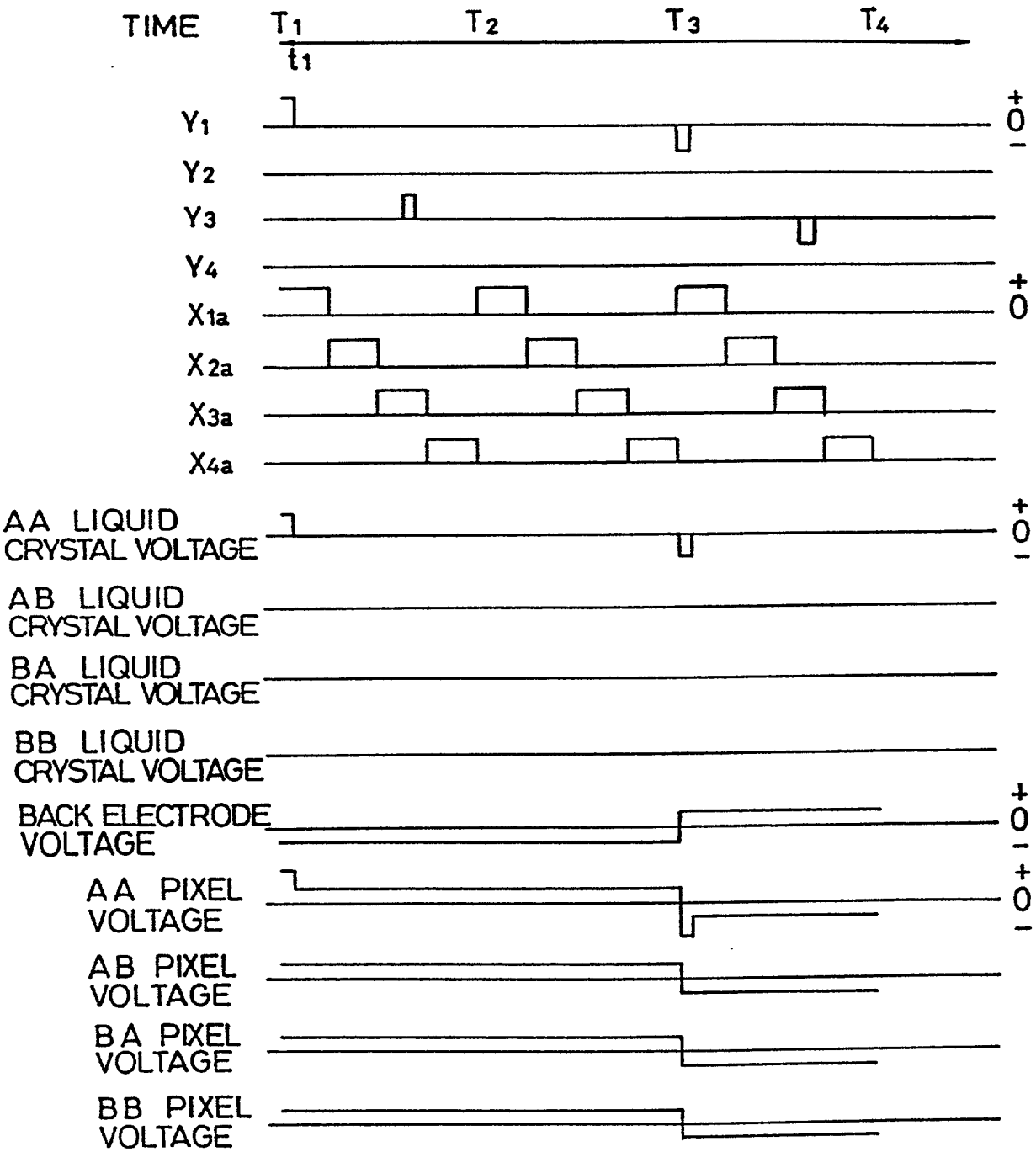


FIG. 18


TIME
T1
T2
T3
T4
t1
Y1
Y2
Y3
Y4
X1a
X2a
X3a
X4a
+
0
−
AA LIQUID CRYSTAL VOLTAGE
AB LIQUID CRYSTAL VOLTAGE
BA LIQUID CRYSTAL VOLTAGE
BB LIQUID CRYSTAL VOLTAGE
BACK ELECTRODE VOLTAGE
AA PIXEL VOLTAGE
AB PIXEL VOLTAGE
BA PIXEL VOLTAGE
BB PIXEL VOLTAGE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)	
Shunpei YAMAZAKI et al.	)	
Based On Serial No. 08/964,028	)	Art Unit: 2871
Which Was Filed: November 4, 1997	)	Examiner: J. Dudek
For: ELECTRO-OPTICAL DEVICE AND	)	
DRIVING METHOD FOR THE	)	
SAME	)	Date: June 2, 1999

NOTICE OF CHANGE OF ADDRESS

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Effective immediately, please note that the address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102

Telephone (703) 790-9110

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DECLARATION: As a below-named inventor, I hereby declare that: My residence, post office address, and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ELECTRO-OPTICAL DEVICE AND DRIVING METHOD FOR THE SAME the specification of which (check one)

X is attached hereto.

____ was filed on _____ as Appl. Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims as amended by an amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed YES	NO
2-323695 (Number)	JAPAN (Country)	11/26/1990 (Date Filed)	X	
2-415721 (Number)	JAPAN (Country)	12/10/1990 (Date Filed)	X	
(Number)	(Country)	(Date Filed)		

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	Status
(Application Serial No.)	(Filing Date)	Status

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named Inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Daniel W. Sixbey	Reg. No. 20,932	David S. Safran	Reg. No. 27,997	Thomas W. Cole	Reg. No. 28,290
Stuart J. Friedman	Reg. No. 24,312	Joan K. Lawrence	Reg. No. 29,940	Charles D. Levine	Reg. No. 32,477
Charles M. Leedom, Jr.	Reg. No. 26,477	Mark W. Binder	Reg. No. 32,642	Steven P. Weihrouch	Reg. No. 32,829
Gerald J. Ferguson, Jr.	Reg. No. 23,016	Donald R. Studebaker	Reg. No. 32,815		

The undersigned hereby authorize the U.S. attorney or agent named herein to accept and follow instructions from Semiconductor Energy Laboratory Co., Ltd. as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorney or agent named herein will be so notified by the undersigned.

Send correspondence to: Sixbey, Friedman, Leedom and Ferguson
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102

Direct telephone calls to: _____ at (703) 790-9110.

Shunpei YAMAZAKI
Full name of sole or first inventor

Shunpei Yamazaki March 16, 1991
Inventor's Signature Date

21-21, Kitakarasuyama, 7-chome, Setagaya-ku, Tokyo 157 Japan
Residence

Japanese
Citizenship

21-21, Kitakarasuyama, 7-chome, Setagaya-ku, Tokyo 157 Japan
Post Office Address

Akira MASE
Full name of second joint inventor, if any

Akira Mase March 16, 1991
Second Inventor's Signature Date

Terasu Hase, 3-3, 381-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan
Residence

Japanese
Citizenship

Terasu Hase, 3-3, 381-1, Hase, Atsugi-shi, Kanagawa-ken
243 Japan
Post Office Address

Masaaki HIROKI
Full name of third joint inventor

Masaaki Hiroki
Third Inventor's Signature

March 16, 1991
Date

533-13, Shirane, Isehara-shi, Kanagawa-ken 259-11 Japan
Residence

Japanese
Citizenship

533-13, Shirane, Isehara-shi, Kanagawa-ken 259-11 Japan
Post Office Address

Full name of fourth joint inventor, if any

Fourth Inventor's Signature
Date

Residence

Citizenship

Post Office Address

Full name of fifth joint inventor, if any

Fifth Inventor's Signature
Date

Residence

Citizenship

Post Office Address

Full name of sixth joint inventor, if any

Sixth Inventor's Signature
Date

Residence

Citizenship

Post Office Address

Full name of seventh joint inventor, if any

Seventh Inventor's Signature
Date

Residence

Citizenship

Post Office Address